CMS1650S User Manual

LED Driver Control/Keyboard Scanning ASIC
Rev. 1.2

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1. Product Description

1.1 General description

CMS1650S is a special drive and control circuit for LED display with keyboard scanning interface. It is internally integrated with MCU input and output control digital interface, data latch, LED drive, keyboard scanning, brightness adjustment and other circuit. CMS1650S has stable performance, reliable quality and strong anti-interference ability. It can be used in applications that work continuously for 24 hours.

1.2 Features

- Two LED display modes: 8 SEG×4 COM and 7 SEG×4 COM
- The SEG drive current is greater than 25mA, and the COM drive current is greater than 150mA
- Support 8 levels of brightness control
- Keyboard scanning: 7×4bit internal integrated triode drive
- High speed two-wire serial interface
- Built in clock oscillation circuit
- Built in power on reset circuit
- Supply voltage range: 2.8V-5.5V
- DIP16/SOP16 pin package

1.3 Applications

Display drivers for household appliances such as set-top box, air conditioner, DVD/VCD, etc.

1.4 System structure diagram

1.5 Pin allocation

```
          DIG1 ⊏  1          16  ⊐ DP/KP
           SCL ⊏  2          15  ⊐ G/KI7
           SDA ⊏  3          14  ⊐ F/KI6
           GND ⊏  4          13  ⊐ E/KI5
          DIG2 ⊏  5          12  ⊐ D/KI4
          DIG3 ⊏  6          11  ⊐ C/KI3
          DIG4 ⊏  7          10  ⊐ VDD
         A/KI1 ⊏  8           9  ⊐ B/KI2
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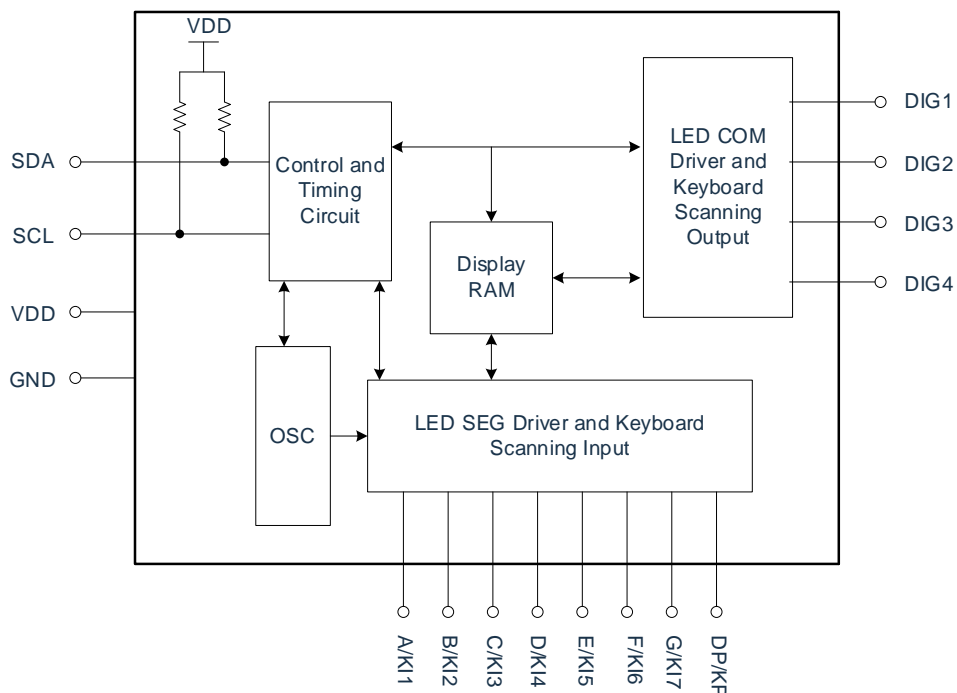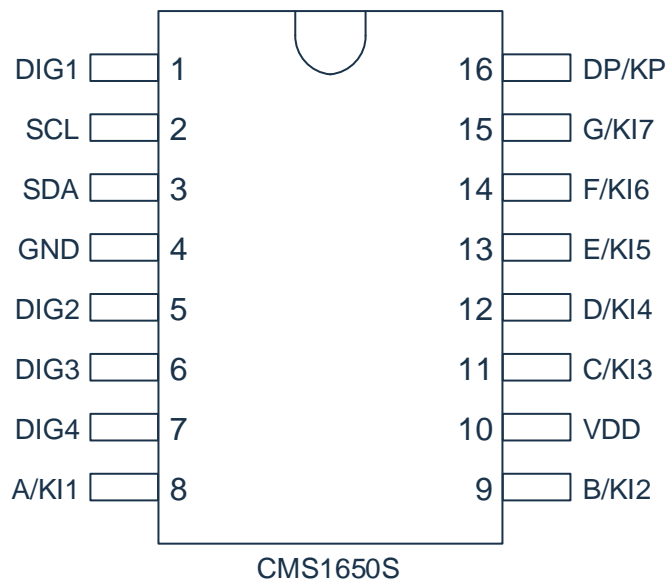
CMS1650S

CMS1650S pin description:

Pin name	Pin number	I/O	Description
DIG1	1	O	LED COM Driver output 1/Keyboard scanning output 1
DIG2	5	O	LED COM Driver output 2/ Keyboard scanning output 2
DIG3	6	O	LED COM Driver output 3/ Keyboard scanning output 3
DIG4	7	O	LED COM Driver output 4/ Keyboard scanning output 4
SCL	2	I	Clock input
SDA	3	O/I	Data input/output
A/KI1	8	O/I	LED SEG Driver output A/ Keyboard scanning input KI1
B/KI2	9	O/I	LED SEG Driver output B/ Keyboard scanning input KI2
C/KI3	11	O/I	LED SEG Driver output C/ Keyboard scanning input KI3
D/KI4	12	O/I	LED SEG Driver output D/ Keyboard scanning input KI4
E/KI5	13	O/I	LED SEG Driver output E/ Keyboard scanning input KI5
F/KI6	14	O/I	LED SEG Driver output F/ Keyboard scanning input KI6
G/KI7	15	O/I	LED SEG Driver output G/ Keyboard scanning input KI7
DP/KP	16	O	LED SEG Driver output DP/ Keyboard scanning output KP
GND	4	-	Logic ground
VDD	10	-	Logic power supply

2. Communication Protocol

CMS1650S uses 2-wire serial transmission protocol to communicate.

1) Start signal (START)/ Stop signal (STOP)

- Start signal: a transition of SDA from a high to a low state while SCL is high. Such as (Figure 2-1) paragraph A.

- Stop signal: a transition of SDA from a low to a high state while SCL is high. Such as (Figure 2-1) paragraph E.

2) ACK signal

CMS1650S will actively pull SDA down after the falling edge of the 8th clock of serial communication, if this communication is correct. Until the rising edge of SCL is detected, SDA is released to the input state (for chips), such as (Figure 2-1) paragraph D.

3) Write "1" and write "0"

- Write "1":   SCL from a low to a high state and then from a high to a low state while SDA is high. Such as (Figure 2-1) paragraph B.

- Write "0":   SCL from a low to a high state and then from a high to a low state while SDA is low. Such as (Figure 2-1) paragraph C.
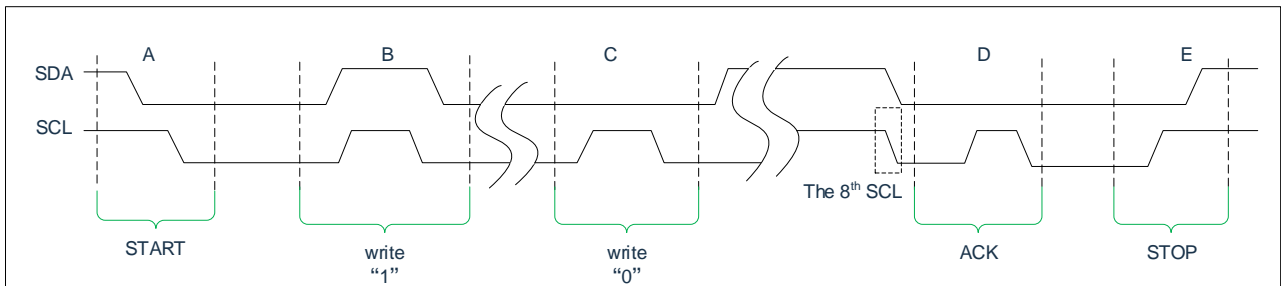
Figure 2-1: CMS1650S communicate protocol

4) One-byte data transmission format

The transmission format of a byte of data is shown in Figure 2-2, where the MSB comes first and the LSB comes second when the data is sent. The data of microprocessor communicates with CMS1650S through two-wire bus interface. The signal on SDA must remain unchanged While SCL is high level; the signal on SDA can be changed only when the clock signal on SCL is low. The starting condition of data input is that SCL is high and SDA changes from a high to a low state; the stopping condition is a transition of SDA from a low to a high state while SCL is high.
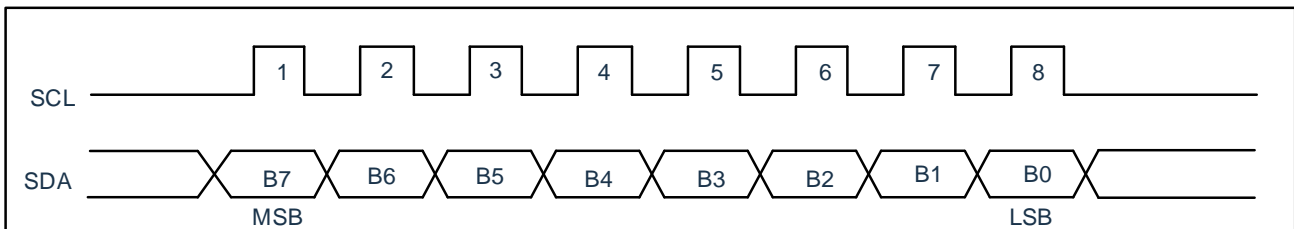
Figure 2-2: Data transmission format

5) Read key data timing

The data is read at the falling edge of SCL and output from CMS1650S SDA pin.
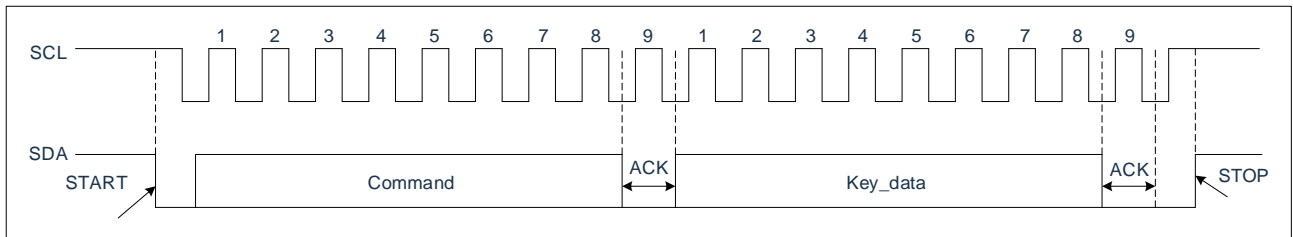
Figure 2-3: Read key data timing

Command: send read key command

Key_data: keyboard scan code read

3. Keyboard Scan Code

CMS1650S corresponding keyboard scan code:

Address	DIG4	DIG3	DIG2	DIG1
A/KI1	47H	46H	45H	44H
B/KI2	4FH	4EH	4DH	4CH
C/KI3	57H	56H	55H	54H
D/KI4	5FH	5EH	5DH	5CH
E/KI5	67H	66H	65H	64H
F/KI6	6FH	6EH	6DH	6CH
G/KI7	77H	76H	75H	74H

Remark: When reading keys, DIG and KI are connected to 2K resistance in series, and key combinations are not supported.

4. Control Command

1) Data command settings

| B7	B6	B5	B4	B3	B2	B1	B0	Description
0	1	0	0	1	0	0	0	Mode command
0	1	0	0	1	X	X	1	Read key data command

Note: The "X" bit in the table can be 1 or 0, recommended to write 0. Other bits must be fixed.

2) Display command settings

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Explain
X	0	0	0		X	X			Level 8 brightness
X	0	0			X	X			Level 1 brightness
X	0	1	0		X	X			Level 2 brightness
X	0	1	1		X	X		Brightness setting	Level 3 brightness
X	1	0	0		X	X			Level 4 brightness
X	1	0	1		X	X			Level 5 brightness
X	1	1	0		X	X			Level 6 brightness
X	1	1	1		X	X			Level 7 brightness
X				0	X	X			8 segment display mode
X				1	X	X			7 segment display mode
X					X	X	0	ON/OFF display bit	Close display
X					X	X	1		Open display

Note: The "X" bit in the table can be 1 or 0, recommended to write 0.

5. Display RAM Address

The register stores the data transmitted from external devices to CMS1650S through a serial interface, with a total of 4-byte units corresponding to the LED lights connected to the chip A/KI~DP/KP and DIG pins respectively. The distribution is shown in the figure below:

Writing LED display data from high to low bytes according to the display address.

A/KI1	B/KI2	C/KI3	D/KI4	E/KI5	F/KI6		G/KI7	DP/KP	
xxHL (the low four bits)					xxHU (the high four bits)				
B0	B1	B2	B4	B5	B6		B7	B8	
68HL					68HU				DIG1
6AHL					6AHU				DIG2
6CHL					6CHU				DIG3
6EHL					6EHU				DIG4

1) Display RAM address command

MSB   LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display RAM address
0	1	1	0	1	0	0	0	68H
0	1	1	0	1	0	1	0	6AH
0	1	1	0	1	1	0	0	6CH
0	1	1	0	1	1	1	0	6EH

Note: This command is used to set the address of the display register.

2) Timing of writing data to display RAM address
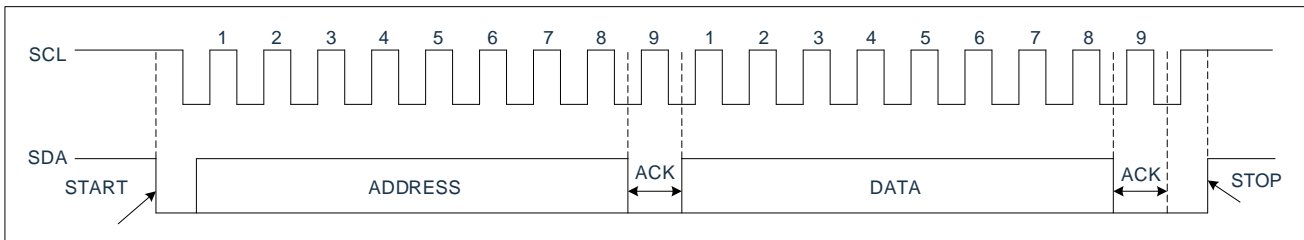
ADDRESS: write display RAM address to CMS1650S.

DATA: write data to CMS1650S for display.

5.1 A complete write display timing
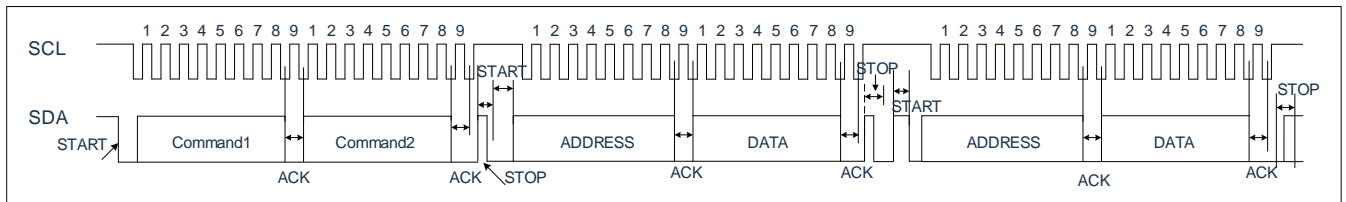
Command1: data command: 48H.

Command2: turn on display and select display brightness level.

ADDRESS: display RAM address.

DATA: display data.

6. Application Circuits

The CMS1650S wiring circuit diagram of driving common cathode digital screen is as follows.
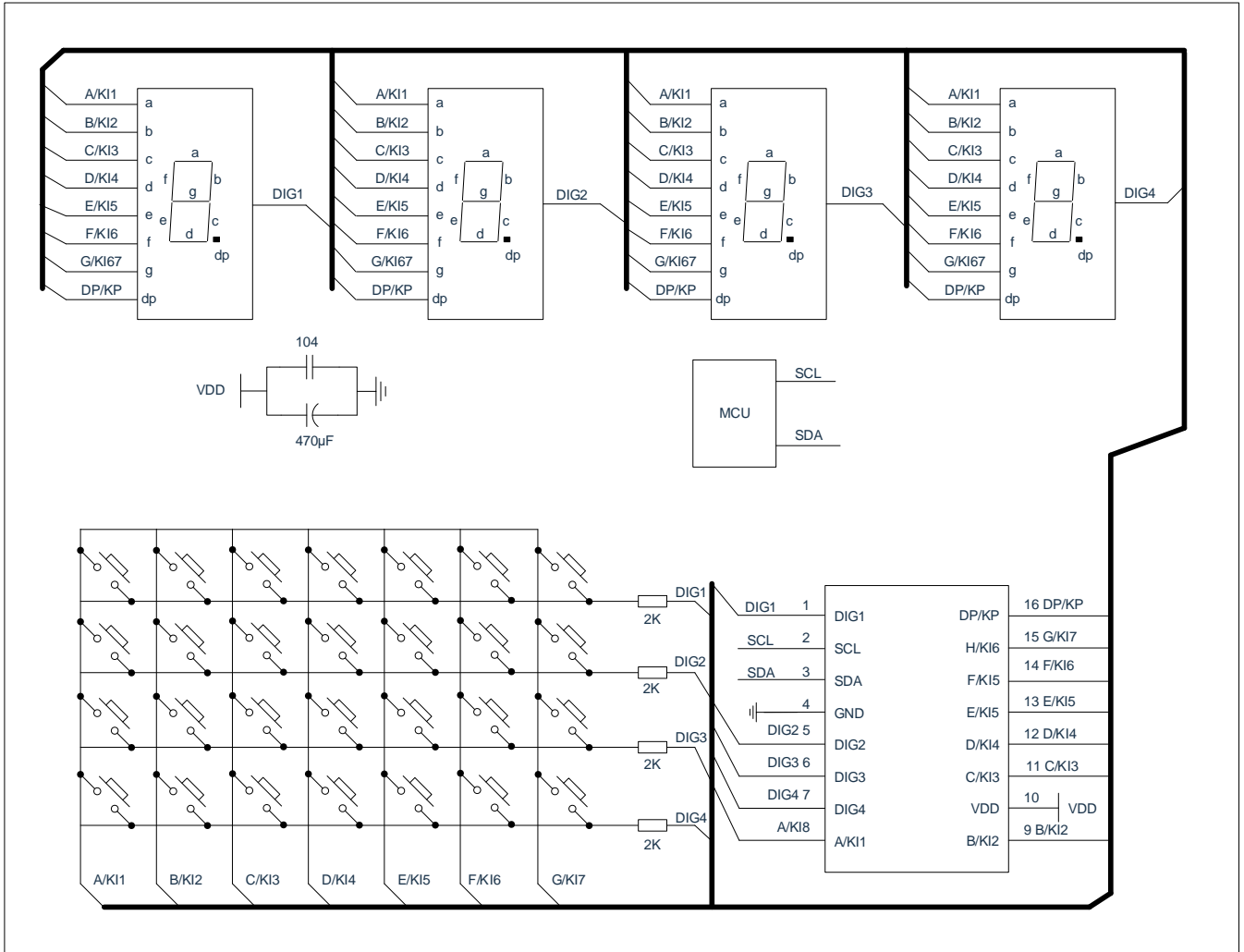
Note:

1) The filter capacitor of the chip should be placed as close to the CMS1650S pin as possible to enhance the filtering.

2) The line width of chip power supply and ground network shall be widened as much as possible during wiring. Two 100pf capacitors connected to the SCL and SDA communication ports can reduce the interference to the communication port.

3) Because the on-voltage drop of Blu-ray digital tubes is about 3.0V, the power supply of CMS1650S should be 5.0V.

7. Electrical Parameter

7.1　Absolute maximum ratings

Symbol	Parameter		Range	Unit
VDD	Supply voltage		-0.5～+7.0	V
VIN	Logic input voltage range	SDA,SCL	-0.5～VDD+0.5V	V
Topr	Working temperature		-40～+85	˚C
Tstg	Storage temperature		-55～+125	˚C
ESD	Human mode (HBM)		3000	V
	Machine mode (MM)		200	V

Note:

1) Stresses above those listed under the Absolute Maximum Ratings section may cause permanent damage to the device. Exposure above maximum rating conditions for extended periods may affect device reliability. It is not recommended that the chip operate beyond these limit parameters under any other conditions.

2) All voltage averages are tested relative to the network ground.

7.2　Range of recommended working conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD	Working voltage	-	2.8	5.0	7.0	V
VIH	High level input voltage	-	0.7VDD	-	VDD	V
VIL	Low level input voltage	-	0	-	0.3VDD	V
TA	Working ambient temperature range	-	-40		+85	˚C
TJ	Working junction temperature range	-	-40		+125	˚C

7.3 DC characteristics

Test at VDD=3.0V~5.5V and -40°C~+85°C, (the voltage during the test is VDD=5.0V and TA=+25°C) unless otherwise indicated.

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD	Working voltage		2.8	5.0	7.0	V
IDD	Working current		0.2		150	mA
IC$_S$	Static current	SCL,SDA,KP are high		0.2		mA
VIL	Low level input voltage				0.5	V
VIH	High level input voltage		3			V
VOH	High level output voltage		VDD-0.4		VDD	V
VOL	Low level output voltage				0.3	V
IOLdig	DIG pin low level output current	VDD=5V, Vo=0.3*VDD		210		mA
		VDD=5V, Vo=0.3V		61		mA
IOHdig	DIG pin high level output current	VDD=5V, Vo=0.7*VDD		18		mA
IOLseg	SEG pin low level output current A~DP	VDD=5V, Vo=0.3*VDD		52		mA
IOHseg	SEG pin high level output current A~DP	VDD=5V, Vo=0.7*VDD		30		mA
		VDD=5V, Vo=VDD-3		46		mA
Rup	KI pin input pull-down resistance	VDD=5V, Vo=0.5*VDD		20		KΩ
	SCL/SDA pull-up resistance	VDD=5V, Vo=0.5*VDD		13		KΩ
VR	Default voltage threshold for power-on reset			2.5		V

7.4 Internal timing parameters

(Test conditions: VDD=5V, T$_A$= 25°C, unless otherwise indicated)

Symbol	Parameter	Min	Typ	Max	Unit
TPR	Reset time generated by power-on detection	10	30	60	ms
TP	Display scan period		7		ms
TKS	Keyboard scan interval, key response time		40		ms

7.5   Interface timing parameters

(Test conditions: VDD=5V, T_A= 25°C)

| Symbol	Parameter	Min	Typ	Max	Unit
TSSTA	SDA establishment time of falling edge start signal	100			ns
THSTA	SDA holding time of falling edge start signal	100			ns
TSST0	SDA establishment time of rising edge stop signal	100			ns
THST0	SDA holding time of rising edge stop signal	100			ns
TCLOW	SCL clock signal low level width	100			ns
TCHIG	SCL clock signal high level width	100			ns
TSDA	Establishment time of SDA input data to the rising edge of SCL	100			ns
THDA	Holding time of SDA input data to the rising edge of SCL	100			ns
TAA	Delay time of SDA output data valid for SCL falling edge	100			ns
TDH	Delay time of SDA output data invalid for SCL falling edge	100			ns
Rate	Average data transfer rate			4M	bps

Note: The unit of measurement in this table in nanoseconds (10^{-9}). If the maximum value is not specified, the theoretical value can be infinite.

8. Packaging

8.1   SOP16
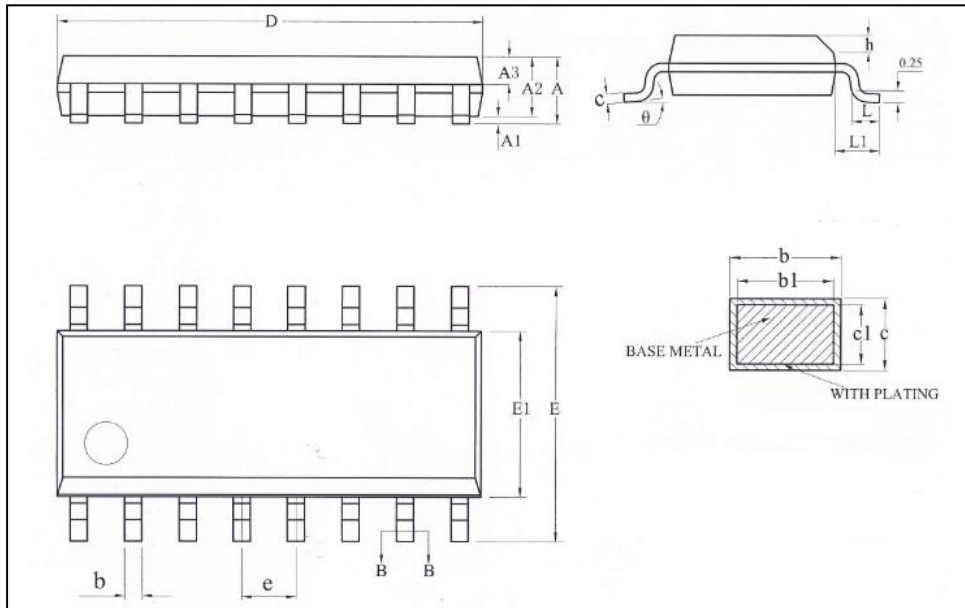
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

8.2 DIP16
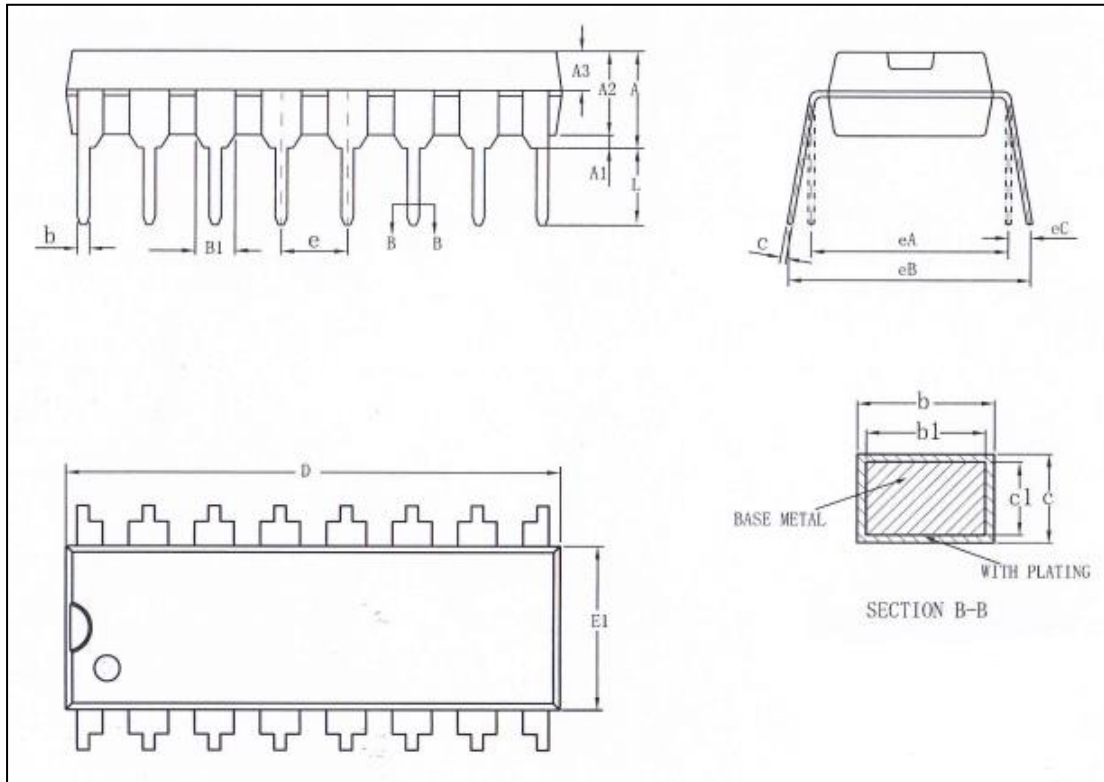
Symbol	Millimeter		
	Min	Nom	Max
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
b	0.44	-	0.52
b1	0.43	0.46	0.49
B1	1.52REF		
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	19.00	19.10	19.20
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	-	9.30
eC	0	-	0.84
L	3.00	-	-

9. Revision History

Version	Date	Revision content
V1.0	May 2019	Initial version
V1.1	November 2021	Updated the format
V1.2	March 2022	Revised "Read key data commands" in Chanpter 4 Control Command 1) Data command settings.