CMS80F761x1 Datasheet

Enhanced flash 8-bit 1T 8051 microcontroller

Rev.1.00

1. Product Features

1.1 Features

- **Compatible with mcS-51's 1T command system**
  - The system clock frequency supports up to 48 MHz
  - The machine cycle is supported up to 1T_{SYS} @ F_{SYS}≤24MHz
  - The fastest machine cycle supports 2T_{SYS} @ F_{SYS}= 48MHz
- **memory**
  - Program FLASH: 64K×8Bit
  - Data FLASH：1K×8Bit
  - General RAM: 256×8Bit
  - Universal XRAM: 4K×8Bit
  - Support BOOT region, 1K/2K/4K optional
  - The program FLASH supports partition protection
- **4 oscillation modes**
  - HSI - Internal high-speed oscillation: 48MHz
  - HSE - External high-speed oscillation: 8MHz/16MHz
  - LSE-External low-speed oscillation: 32.768KHz
  - LSI-Internal low-speed oscillation: 125KHz
- **GPIO**
  - Up to 30 GPIOs
  - Both support pull-up/down resistor function
  - Both support edge (rising/falling/double-edge) interrupts
  - Both support wake-up function
- **Interrupt source**
  - All external port interrupts are supported
  - 8 timer interrupts
  - Other peripheral interrupts
- **timer**
  - WDT Timer (Watchdog Timer)
  - WWDT timer (window watchdog timer).
  - Timer0/1，Timer2，Timer3/4
  - LSE_Timer (supports sleep wake-up function).
  - WUT (wake-up timer)
  - BRT (Serial Port Baud Rate Clock Generator)
- **Cyclic redundancy check cell**
  - CRC16 (CRC16-CCITT)
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **PWM**
  - 6-channel PWM
  - 6 mutually independent cycle counters
  - Supports independent/complementary/synchronous/grouped modes
  - Edge alignment is supported
  - Supports complementary mode dead-zone delay function
- **Operating voltage range**
  - 2.1V~5.5V
- **Operating temperature range**
  - -40℃~105℃
- **Low Voltage Reset Function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low Voltage Detection Function (LVD)**
  - 2.0V~4.3V 8 levels selectable
- **High Precision 12-bit ADC**
  - Up to 30 AD external channels
  - Reference Voltage Selectable (1.2V/2.0V/2.4V/3.0V/VDD)
  - detectable Internal 1.2V reference voltage
  - Supports hardware-triggered start conversion features
  - Supports a set of result number comparison functions
- **High sensitivity touch**
- **Hardware LCD driver**
  - Duty cycle 1/4, 1/5, 1/6, 1/8 selectable
  - Three clock sources are available, LSI/LSE/system clock
  - Conventional resistive LCD, 1/2, 1/3, 1/4 BIAS selectable
  - Supports working in sleep mode
  - Supports fast charging mode
  - Support energy-saving mode, resistive voltage divider 60K/225K/900K selectable
  - Supports up to 4COM x 23SEG, 5COM x 22SEG 6COM x 21SEG、8COM x 19SEG
- **Hardware LED matrix driver**
  - Duty cycle 1/4, 1/5, 1/6, 1/8 selectable
  - Supports two modes of common-negative/common-positive
  - Three clock sources are available, LSI/LSE/system clock
  - COM, SEG current selectable
  - Supports up to 4COM x 20SEG, 5COM x 19SEG 6COM x18SEG、8COM x16SEG
- **Hardware LED dot matrix driver**
  - Three clock sources are available, LSI/LSE/system clock
  - Supports both cyclic and interrupt scan
  - Supports each lamp display data configurable
  - Supports two on-time options per lamp
  - Current 16 steps selectable
  - Supports up to 8 pin drivers and up to 56 lamp drivers

    Choose from dot matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8

- **Communication module**
  - 1xSPI (communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - 3xUART (baud rate up to 1Mb/s).
    UART1 can be mapped arbitrarily by GPIO
- **Low-power mode**
  - Idle mode (IDLE)
  - Sleep Mode (STOP)
- **Supports 96-bit unique ID number (UID)**
  - Each chip has a separate ID number
- **Supports two-wire serial programming and debugging**

1.2 Product comparison

Peripheral interface \ Product		CMS80F76161	CMS80F76171	CMS80F76181	CMS80F76191
Maximum clock frequency		48MHz			
Storage Module	APROM	64/63/62/60 KB(1)			
	BOOT	0/1/2/4 KB(1)			
	Data FLASH	1 KB			
	RAM	256 B			
	XRAM	4 KB			
timer	WDT	1			
	WWDT	1			
	Timer0/1	2 (16bit)			
	Timer2	1 (16bit)			
	Timer3/4	2 (16bit)			
	LSE_Timer	1 (16bit)			
	WUT	1 (12bit)			
	BRT	1 (16bit)			
Enhanced Digital peripherals	CRC	CRC16-CCITT			
	BUZZER	1			
	PWM	6(16bit)			
Displays the interface	LED matrix	4COMx14SEG 5COMx13SEG 6COMx12SEG 8COMx10SEG	4COMx16SEG 5COMx15SEG 6COMx14SEG 8COMx12SEG	4COMx18SEG 5COMx17SEG 6COMx16SEG 8COMx14SEG	4COMx20SEG 5COMx19SEG 6COMx18SEG 8COMx16SEG
	LED dot matrix	4x4、5x5、6x6、6x7、7x7、7x8			
	LCD	4COMx14SEG 5COMx13SEG 6COMx12SEG 8COMx10SEG	4COMx18SEG 5COMx17SEG 6COMx16SEG 8COMx14SEG	4COMx22SEG 5COMx21SEG 6COMx20SEG 8COMx18SEG	4COMx23 5COMx22SEG 6COMx21SEG 8COMx19SEG
Communication module	SPI	1			
	I2C	1			
	UART	3			
Analog module	12bit-ADC (Number of external channels)	18	22	26	30
	TOUCH	18	22	26	30
GPIOs		18	22	26	30
LVR		1.8V/2.0V/2.5V/3.5V			
LVD		2.0~4.6V, 8 levels			
Operating voltage		2.1~5.5 V			
Operating temperature		-40~105℃			
packaging		SOP20/TSSOP20	SOP24	SOP28	LQFP32

Note: (1) The SIZE OF THE APROM and BOOT space is set through the system configuration register, and the maximum total of APROM and BOOT space is 64K.

2. System Overview

2.1 System Introduction

The series is an 8051 core, MCS-51 compatible 1T command system, a general-purpose IO type 8-bit chip, operating frequency up to 48MHz, the MCU has the following features:

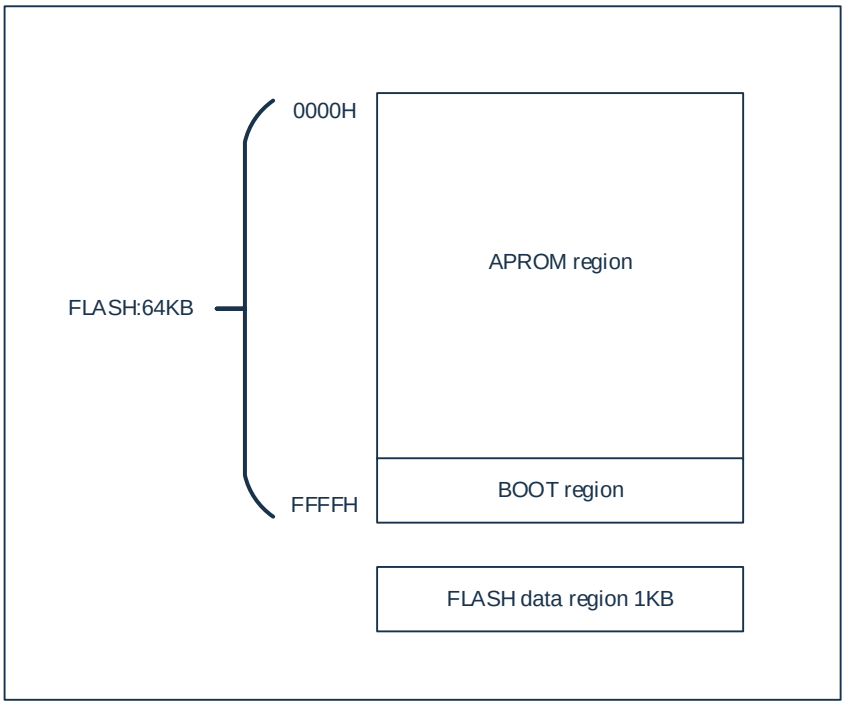
- Features a maximum of 64KB of program area, 256B of RAM space, 4KB of XRAM, and 1KB of non-volatile data area.
- With four oscillation modes, the system clock can be freely switched between three clock sources (HSE and LSE are prohibited from switching to each other), and external oscillator stop detection.
- Support normal, idle, sleep three working modes, can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage monitoring LVD, watchdog, window watchdog overflow reset and other protection settings can effectively improve the reliability of system operation.
- It has a variety of interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, which can respond to external events in a timely manner and improve the utilization of MCUs.
- Up to 10 timers, can achieve timing, counting, input capture, output comparison, timed wake-up, baud rate generator and other functions.
- Has a cyclic redundancy check unit CRC.
- UP to 8COM and 20SEG LED matrix drivers, 7x 8 LED dot matrix drivers.
- UP to 8COM and 23SEG LCD driver modules.
- Six 16-bit PWMs support independent, complementary, synchronous three modes of output, while with dead-zone control function.
- With 1 I2C, 1 SPI, 3 UART communication modules, it can realize data transmission between the system and other devices.
- Features a high accuracy 12-bit ADC with selectable internal reference voltage.
- Touch with high sensitivity.

2.2 Memory Structure

2.2.1 Program Memory FLASH

The chip has a 64KB flash storage space, and the APROM area and the BOOT area share the entire FLASH space.

The flash space allocation block diagram is as follows:

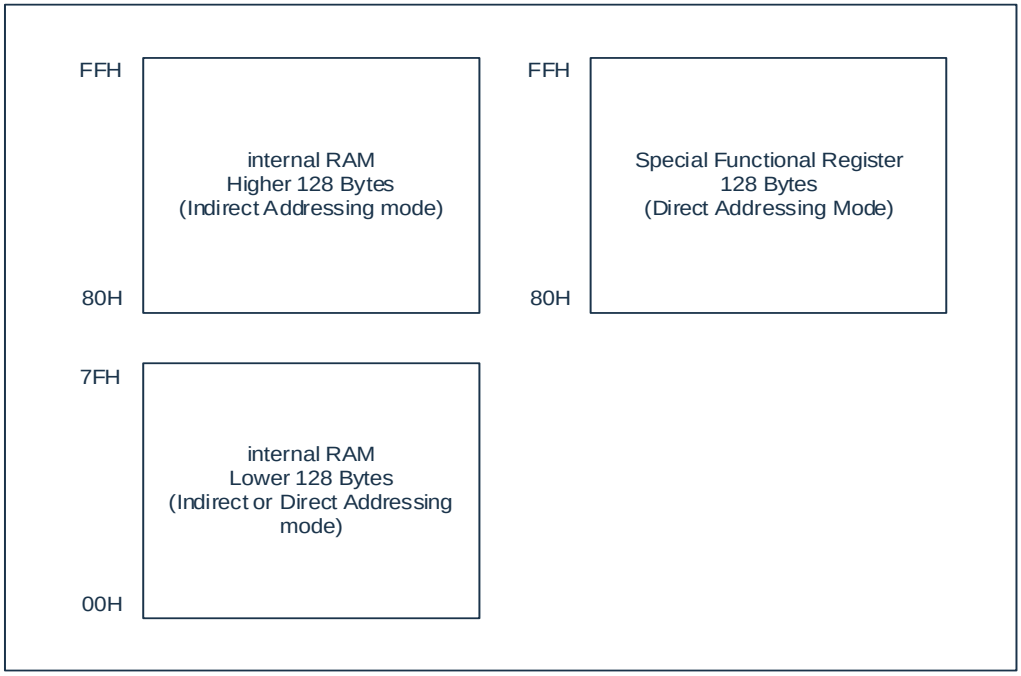


The size of the BOOT can be configured as follows:

64K (Program Storage area)				
address space allocation	APROM area		BOOT area	
Mode 0	64K	0000H-FFFFH	--	--
Mode 1	63K	0000H-FBFFH	1K	FC00H-FFFFH
Mode 2	62K	0000H-F7FFH	2K	F800H-FFFFH
Mode 3	60K	0000H-EFFFH	4K	E000H-EFFFH

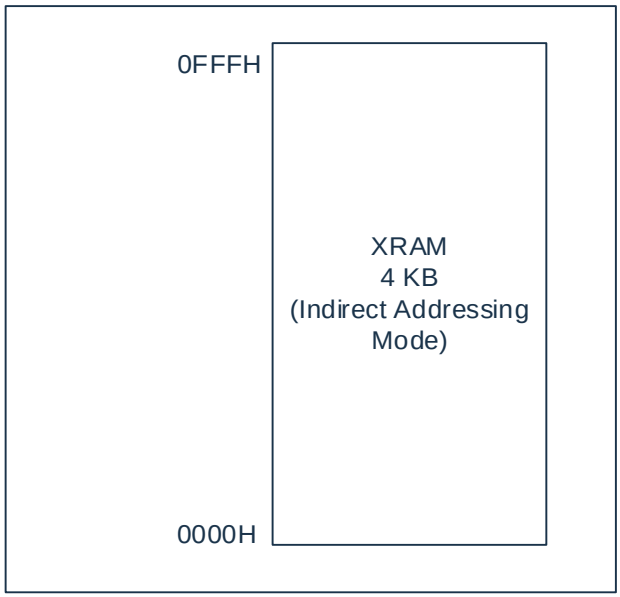
2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The RAM space allocation block diagram is shown in the following figure:



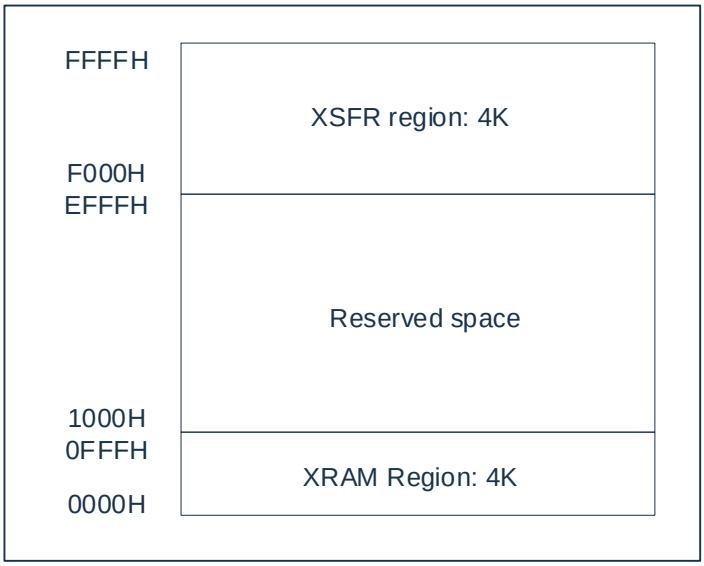
2.2.3 External Data Memory XRAM

There is a 4KB XRAM area inside the chip, which is not connected to RAM/FLASH, and the XRAM space allocation block diagram is shown in the following figure.



2.2.4 Special Function Register XSFR

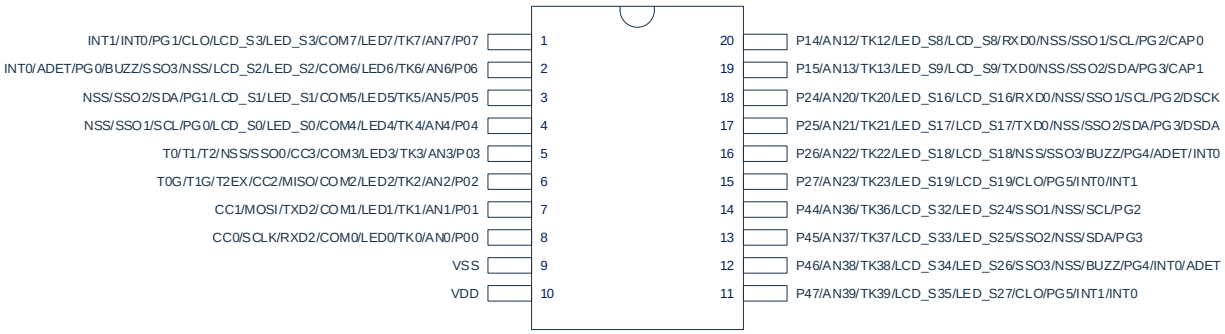
XSFR is a special register shared by the addressing space and XRAM, mainly including: port control registers, other function control registers. Its addressing range is as follows:



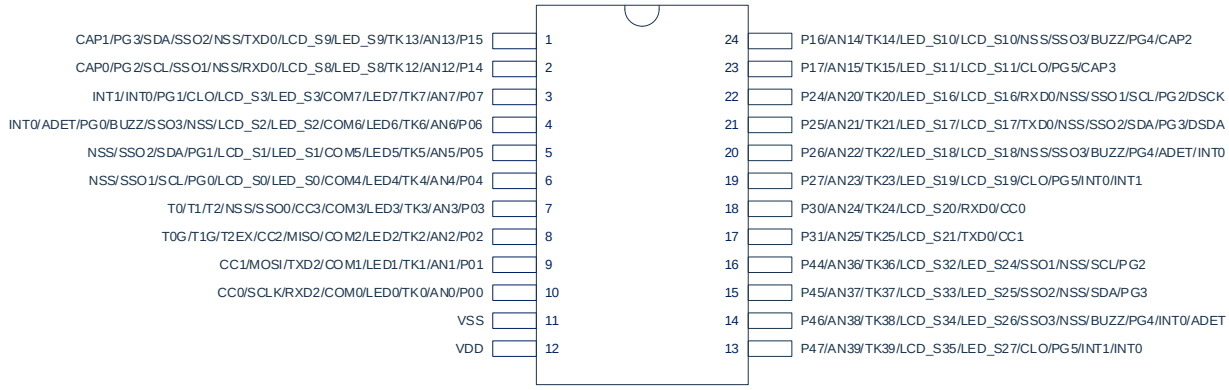
3. Pin Definition

3.1 Pin Description

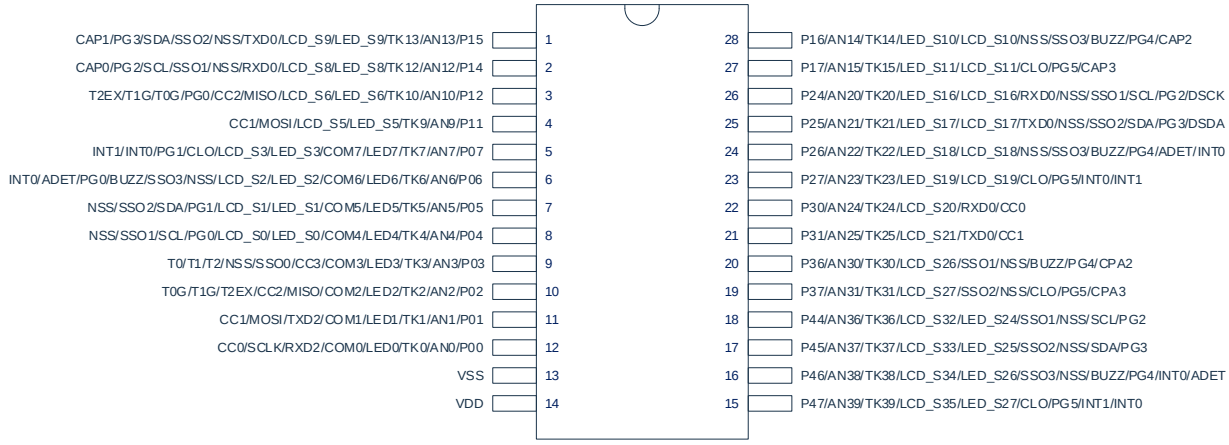
3.1.1 CMS80F76161 Pin Figure -SOP20/TSSOP20



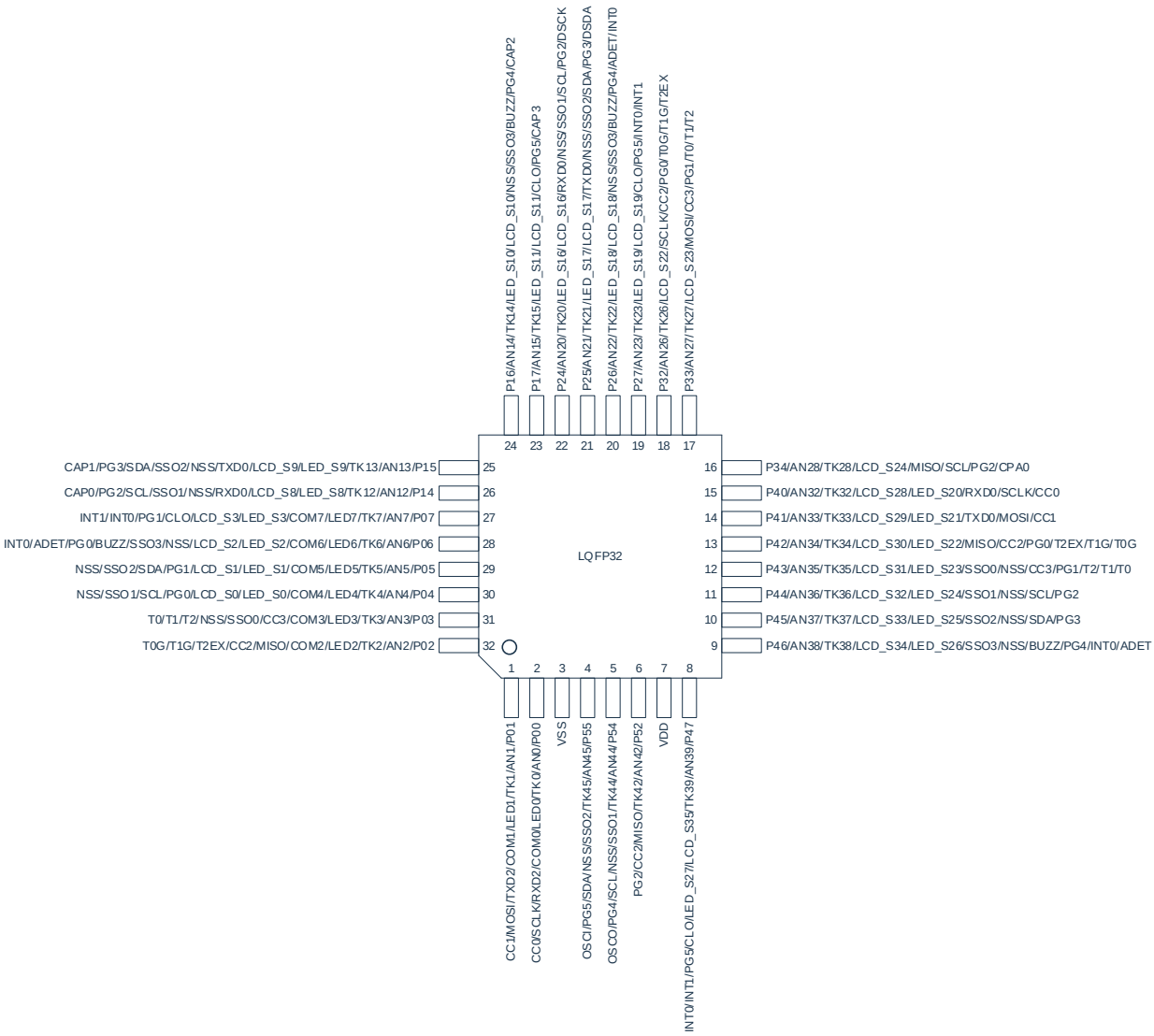
3.1.2 CMS80F76171 Pin Figure-SOP24



3.1.3 CMS80F76181 Pin Figure-SOP28



3.1.4 CMS80F76191 Pin Figure - LQFP32



3.2 Pin Function Description

Symbol description: I/O represents digital input/output, I represents digital input, O represents digital output, AI represents analog input, and AO represents analog output.

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
8	10	12	2	P00	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN0	AI	ADC channel 0 input
				TK0	AI	Touch key channel 0 input
				LED0	O	LED dot matrix scan LED0 output
				COM0	O	LED COM0 output
				RXD2	I/O	UART2 data input/synchronous mode data output
				SCLK	I/O	SPI clock input and output
				CC0	O	Timer2 compare output channel 0
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
7	9	11	1	P01	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN1	AI	ADC channel 1 input
				TK1	AI	Touch key channel 1 input
				LED1	O	LED dot matrix scan LED1 output
				COM1	O	LED COM1 output
				TXD2	O	UART2 data output
				MOSI	I/O	SPI data master sends slave receive
				CC1	O	Timer2 compare output channel 1
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
6	8	10	32	P02	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN2	AI	ADC channel 2 input
				TK2	AI	Touch key channel 2 input
				LED2	O	LED dot matrix scan LED2 output
				WITH2	O	LED COM2 output
				MISO	I/O	The SPI data master receives the

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
						slave send
				CC2	O	Timer2 compare output channel 2
				T2EX	I	Timer2 drops along the auto-reload input
				T1G	I	Timer1 gated input
				T0G	I	Timer0 gated input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
5	7	9	31	P03	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN3	AI	ADC channel 3 input
				TK3	AI	Touch key channel 3 input
				LED3	O	LED dot matrix scans LED3 output
				WITH3	O	LED COM3 output
				CC3	O	Timer2 compare output channel 3
				TXD0	O	UART0 data output
				NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
				T2	I	Timer2 external event or gated input
				T1	I	Timer1 external clock input
				T0	I	Timer0 external clock input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
4	6	8	30	P04	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN4	AI	ADC channel 4 input
				TK4	AI	Touch key channel 4 input
				LED4	O	LED dot matrix scan LED4 output
				WITH4	O	LED COM4 output
				LED_S0	O	LED SEG0 output
				LCD_S0	O	LCD SEG0 output
				PG0	O	PWM channel 0 output
				SCL	I/O	I2C clock input and output
				NSS(NSSO1)	I/O	The SPI is selected from the control

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
						select input/master select 1 output
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
3	5	7	29	P05	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN5	AI	ADC channel 5 input
				TK5	AI	Touch key channel 5 input
				LED5	O	LED dot matrix scans LED5 output
				WITH5	O	LED COM5 output
				LED_S1	O	LED SEG1 output
				LCD_S1	O	LCD SEG1 output
				PG1	O	PWM channel 1 output
				SDA	I/O	I2C data input and output
				NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
2	4	6	28	P06	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN6	AI	ADC channel 6 input
				TK6	AI	Touch key channel 6 input
				LED6	O	LED dot matrix scan LED6 output
				WITH6	O	LED COM6 output
				LED_S2	O	LED SEG2 output
				LCD_S2	O	LCD SEG2 output
				NSS(NSSO3)	I/O	The SPI selects input from the control/main control select 3 output
				BUZZ	O	Buzzer drive output
				PG0	O	PWM channel 0 output
				CUSTOM	I	ADC external trigger input
				INT0	I	External interrupt 0 input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
1	3	5	27	P07	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN7	AI	ADC channel 7 input
				TK7	AI	Touch key channel 7 input
				LED7	O	LED dot matrix scan LED7 output
				WITH7	O	LED COM7 output
				LED_S3	O	LED SEG3 output
				LCD_S3	O	LCD SEG3 output
				CLO	O	System clock divider output
				PG1	O	PWM channel 1 output
				INT0	I	External interrupt 0 input
				INT1	I	External interrupt 1 input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	4	-	P11	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN9	AI	ADC channel 9 input
				TK9	AI	Touch key channel 9 input
				LED_S5	O	LED SEG5 output
				LCD_S5	O	LCD SEG5 output
				MOSI	I/O	SPI data master sends slave receive
				CC1	O	Timer2 compare output channel 1
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
-	-	3	-	P12	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN10	AI	ADC channel 10 input
				TK10	AI	Touch key channel 10 input
				LED_S6	O	LED SEG6 output
				LCD_S6	O	LCD SEG6 output
				MISO	I/O	The SPI data master receives the slave send
				CC2	O	Timer2 compare output channel 2

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				PG0	O	PWM channel 0 output
				T0G	I	Timer0 gated input
				T1G	I	Timer1 gated input
				T2EX	I	Timer2 drops along the auto-reload input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
20	2	2	26	P14	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN12	AI	ADC channel 12 inputs
				TK12	AI	Touch key channel 12 input
				LED_S8	O	LED SEG8 output
				LCD_S8	O	LCD SEG8 output
				RXD0	I/O	UART0 data input/synchronous mode data output
				NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
				SCL	I/O	^{I2C}clock input and output
				PG2	O	PWM channel 2 output
				CAP0	I	Timer2 input capture channel 0
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
19	1	1	25	P15	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN13	AI	ADC channel 13 input
				TK13	AI	Touch key channel 13 input
				LED_S9	O	LED SEG9 output
				LCD_S9	O	LCD SEG9 output
				TXD0	O	UART0 data output
				NSS(NSSO2)	I/O	The SPI selects input from the control/ main control select 2 output
				SDA	I/O	I2C data input and output
				PG3	O	PWM channel 3 output
				CAP1	I	Timer2 input capture channel 1

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
-	24	28	24	P16	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN14	AI	ADC channel 14 inputs
				TK14	AI	Touch key channel 14 input
				LED_S10	O	LED SEG10 output
				LCD_S10	O	LC DSEG10 output
				NSS(NSSO3)	I/O	The SPI selects input from the control/main control select 3 output
				BUZZ	O	Buzzer drive output
				PG4	O	PWM channel 4 output
				CAP2	I	Timer2 input capture channel 2
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	23	27	23	P17	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN15	AI	ADC channel 15 inputs
				TK15	AI	Touch key channel 15 input
				LED_S11	O	LED SEG11 output
				LCD_S11	O	LC DSEG11 output
				CLO	O	System clock divider output
				PG5	O	PWM channel 5 output
				CAP3	I	Timer2 input capture channel 3
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
18	22	26	22	P24	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN20	AI	ADC channel 20 input
				TK20	AI	Touch key channel 20 input
				LED_S16	O	LED SEG16 output
				LCD_S16	O	LC DSEG16 output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				RXD0	I/O	UART0 data input/ synchronous mode data output
				NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
				SCL	I/O	I2C clock input and output
				PG2	O	PWM channel 2 output
				DSCK	I/O	Programming/ debugging clock inputs/outputs
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
17	21	25	21	P25	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN21	AI	ADC channel 20 input
				TK21	AI	Touch key channel 20 input
				LED_S17	O	LED SEG17 output
				LCD_S17	O	LC DSEG17 output
				TXD0	O	UART0 data output
				NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
				SDA	I/O	I2C data input and output
				PG3	O	PWM channel 3 output
				DSDA	I/O	Programming/debugging data input and output ports
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
16	20	24	20	P26	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN22	AI	ADC channel 20 input
				TK22	AI	Touch key channel 20 input
				LED_S18	O	LED SEG18 output
				LCD_S18	O	LC DSEG18 output
				NSS(NSSO3)	I/O	The SPI selects input from the control/main control select 3 output
				BUZZ	O	Buzzer drive output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				PG4	O	PWM channel 4 output
				CUSTOM	I	ADC external trigger input
				INT0	I	External interrupt 0 input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
15	19	23	19	P27	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN23	AI	ADC channel 23 input
				TK23	AI	Touch key channel 23 input
				LED_S19	O	LED SEG19 output
				LCD_S19	O	LCD SEG19 output
				CLO	O	System clock divider output
				PG5	O	PWM channel 5 output
				INT0	I	External interrupt 0 input
				INT1	I	External interrupt 1 input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	18	22	-	P30	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN24	AI	ADC channel 24 input
				TK24	AI	Touch key channel 24 input
				LCD_S20	O	LCD SEG20 output
				RXD0	I/O	UART0 data input/synchronous mode data output
				CC0	O	Timer2 compare output channel 0
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	17	21	-	P31	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN25	AI	ADC channel 25 input
				TK25	AI	Touch key channel 25 input
				LCD_S21	O	LCD SEG21 output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				TXD0	O	UART0 data output
				CC1	O	Timer2 compare output channel 1
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
-	-	-	18	P32	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN26	AI	ADC channel 26 input
				TK26	AI	Touch key channel 26 input
				LCD_S22	O	LCD SEG22 output
				SCLK	I/O	SPI clock input and output
				CC2	O	Timer2 compare output channel 2
				PG0	O	PWM channel 0 output
				T0G	I	Timer0 gated input
				T1G	I	Timer1 gated input
				T2EX	I	Timer2 drops along the auto-reload input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
-	-	-	17	P33	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN27	AI	ADC channel 27 input
				TK27	AI	Touch key channel 27 input
				LCD_S23	O	LCD SEG23 output
				MOSI	I/O	SPI data master sends slave receive
				CC3	O	Timer2 compare output channel 3
				PG1	O	PWM channel 1 output
				T0	I	Timer0 external clock input
				T1	I	Timer1 external clock input
				T2	I	Timer2 external event or gated input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	16	P34	I/O	GPIO configure input and output through registers, pull up, pull down

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
						and other functions
				AN28	AI	ADC channel 28 input
				TK28	AI	Touch key channel 28 input
				LCD_S24	O	LCD SEG24 output
				MISO	I/O	The SPI data master receives the slave send
				SCL	I/O	I2C clock input and output
				PG2	O	PWM channel 2 output
				CAP0	I	Timer2 input capture channel 0
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	20	-	P36	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN30	AI	ADC channel 30 input
				TK30	AI	Touch key channel 30 input
				LCD_S26	O	LCD SEG26 output
				NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
				BUZZ	O	Buzzer drive output
				PG4	O	PWM channel 4 output
				CAP2	I	Timer2 input capture channel 2
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/ synchronous mode data output
-	-	19	-	P37	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN31	AI	ADC channel 31 input
				TK31	AI	Touch key channel 31 input
				LCD_S27	O	LCD SEG27 output
				NSS(NSSO2)	I/O	The SPI selects input from the control/main control select 2 output
				CLO	O	System clock divider output
				PG5	O	PWM channel 5 output
				CAP3	I	Timer2 input capture channel 3
				TXD1	O	UART1 data output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	15	P40	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN32	AI	ADC channel 32 input
				TK32	AI	Touch key channel 32 input
				LCD_S28	O	LCD SEG28 output
				LED_S20	O	LED SEG20 output
				RXD0	I/O	UART0 data input/synchronous mode data output
				SCLK	I/O	SPI clock input and output
				CC0	O	Timer2 compare output channel 0
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	14	P41	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN33	AI	ADC channel 32 input
				TK33	AI	Touch key channel 32 input
				LCD_S29	O	LCD SEG29 output
				LED_S21	O	LED SEG21 output
				TXD0	O	UART0 data output
				MOSI	I/O	SPI data master sends slave receive
				CC1	O	Timer2 compare output channel 1
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
	-	-	13	P42	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN34	AI	ADC channel 34 input
				TK34	AI	Touch key channel 34 input
				LCD_S30	O	LCD SEG30 output
				LED_S22	O	LED SEG22 output
				MISO	I/O	The SPI data master receives the slave send

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				CC2	O	Timer2 compare output channel 2
				PG0	O	PWM channel 0 output
				T2EX	I	Timer2 drops along the auto-reload input
				T1G	I	Timer1 gated input
				T0G	I	Timer0 gated input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	12	P43	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN35	AI	ADC channel 35 input
				TK35	AI	Touch key channel 35 input
				LCD_S31	O	LCD SEG31 output
				LED_S23	O	LED SEG23 output
				NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
				CC3	O	Timer2 compare output channel 3
				PG1	O	PWM channel 1 output
				T2	I	Timer2 external event or gated input
				T1	I	Timer1 external clock input
				T0	I	Timer0 external clock input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
14	16	18	11	P44	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN36	AI	ADC channel 36 input
				TK36	AI	Touch key channel 36 input
				LCD_S32	O	LCD SEG32 output
				LED_S24	O	LED SEG24 output
				NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
				SCL	I/O	I2C clock input and output
				PG2	O	PWM channel 2 output
				TXD1	O	UART1 data output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				RXD1	I/O	UART1 data input/synchronous mode data output
13	15	17	10	P45	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN37	AI	ADC channel 37 input
				TK37	AI	Touch key channel 37 input
				LCD_S33	O	LCD SEG33 output
				LED_S25	O	LED SEG25 output
				NSS(NSSO2)	I/O	The SPI is selected from the control select input/master select 1 output
				SDA	I/O	I2C data input and output
				PG3	O	PWM channel 3 output
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
12	14	16	9	P46	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN38	AI	ADC channel 38 input
				TK38	AI	Touch key channel 38 input
				LCD_S34	O	LCD SEG34 output
				LED_S26	O	LED SEG26 output
				NSS(NSSO3)	I/O	The SPI is selected from the control select input/master select 1 output
				BUZZ	O	Buzzer drive output
				PG4	O	PWM channel 4 output
				INT0	I	External interrupt 0 input
				CUSTOM	I	ADC external trigger input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
11	13	15	8	P47	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN39	AI	ADC channel 39 input
				TK39	AI	Touch key channel 39 input
				LCD_S35	O	LCD SEG35 output

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				LED_S27	O	LED SEG27 output
				CLO	O	System clock divider output
				PG5	O	PWM channel 5 output
				INT1	I	External interrupt 1 input
				INT0	I	External interrupt 0 input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	6	P52	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN42	AI	ADC channel 42 input
				TK42	AI	Touch key channel 42 input
				MISO	I/O	The SPI data master receives the slave send
				CC2	O	Timer2 compare output channel 2
				PG2	O	PWM channel 2 output
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	5	P54	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN44	AI	ADC channel 44 input
				TK44	AI	Touch key channel 44 input
				NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
				SCL	I/O	I2C clock input and output
				PG4	O	PWM channel 4 output
				OSCO	AO	External oscillation HSE/LSE output
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
-	-	-	4	P55	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
				AN45	AI	ADC channel 45 input
				TK45	AI	Touch key channel 45 input

Pin number				Pin name	Pin type	description
SOP20/ TSSOP20	SOP24	SOP28	LQFP32			
				NSS(NSSO2)	I/O	The SPI is selected from the control select input/master select 1 output
				SDA	I/O	I2C data input and output
				PG5	O	PWM channel 5 output
				OSCI	AI	External oscillation HSE/LSE input
				TXD1	O	UART1 data output
				RXD1	I/O	UART1 data input/synchronous mode data output
9	11	13	3	VSS	P	Grounding feet
10	12	14	7	VDD	P	Supply voltage input pin

3.3 GPIO features

Pins are shared in a variety of functions, and each I/O port can be flexibly configured with digital functions or specified analog functions. I/O as a universal GPIO port has the following characteristics:

- 2 levels I/O output slope can be configured.
- Data latch status or pin status can be read.
- Configurable rising, falling, and dual edge trigger interrupts.
- Configurable rising, falling, and dual-edge interrupt wake-up chip.
- It can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 List of pin functions

List of digital function ports:

	External input	Digital function configuration							
		0	1	2	3	4	5	6	7
P00	-	GPIO	ANA	RXD2	SCLK	CC0	-	TXD1	RXD1
P01	-	GPIO	ANA	TXD2	MOSI	CC1	-	TXD1	RXD1
P02	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	-	TXD1	RXD1
P03	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	-	TXD1	RXD1
P04	-	GPIO	ANA	-	NSS(NSSO1)	SCL	PG0	TXD1	RXD1
P05	-	GPIO	ANA	-	NSS(NSSO2)	SDA	PG1	TXD1	RXD1
P06	MOQ/INT0	GPIO	ANA	-	NSS(NSSO3)	BUZZ	PG0	TXD1	RXD1
P07	INT0/INT1	GPIO	ANA	-	-	CLO	PG1	TXD1	RXD1
P11	-	GPIO	ANA	-	MOSI	CC1	-	TXD1	RXD1
P12	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG0	TXD1	RXD1
P14	CAP0	GPIO	ANA	RXD0	NSS(NSSO1)	SCL	PG2	TXD1	RXD1
P15	CAP1	GPIO	ANA	TXD0	NSS(NSSO2)	SDA	PG3	TXD1	RXD1
P16	CAP2	GPIO	ANA	-	NSS(NSSO3)	BUZZ	PG4	TXD1	RXD1
P17	CAP3	GPIO	ANA	-	-	CLO	PG5	TXD1	RXD1
P24	DSCK	GPIO	ANA	RXD0	NSS(NSSO1)	SCL	PG2	TXD1	RXD1
P25	DSDA	GPIO	ANA	TXD0	NSS(NSSO2)	SDA	PG3	TXD1	RXD1
P26	MOQ/INT0	GPIO	ANA	-	NSS(NSSO3)	BUZZ	PG4	TXD1	RXD1
P27	INT0/INT1	GPIO	ANA	-	-	CLO	PG5	TXD1	RXD1
P30	-	GPIO	ANA	RXD0	-	CC0	-	TXD1	RXD1
P31	-	GPIO	ANA	TXD0	-	CC1	-	TXD1	RXD1
P32	T0G/T1G/T2EX	GPIO	ANA	-	SCLK	CC2	PG0	TXD1	RXD1
P33	T0/T1/T2	GPIO	ANA	-	MOSI	CC3	PG1	TXD1	RXD1
P34	CAP0	GPIO	ANA	-	MISO	SCL	PG2	TXD1	RXD1
P36	CAP2	GPIO	ANA		NSS(NSSO1)	BUZZ	PG4	TXD1	RXD1
P37	CAP3	GPIO	ANA		NSS(NSSO2)	CLO	PG5	TXD1	RXD1
P40	-	GPIO	ANA	RXD0	SCLK	CC0	-	TXD1	RXD1
P41	-	GPIO	ANA	TXD0	MOSI	CC1	-	TXD1	RXD1
P42	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG0	TXD1	RXD1
P43	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	PG1	TXD1	RXD1
P44	-	GPIO	ANA	-	NSS(NSSO1)	SCL	PG2	TXD1	RXD1
P45	-	GPIO	ANA	-	NSS(NSSO2)	SDA	PG3	TXD1	RXD1
P46	MOQ/INT0	GPIO	ANA	-	NSS(NSSO3)	BUZZ	PG4	TXD1	RXD1
P47	INT0/INT1	GPIO	ANA	-	-	CLO	PG5	TXD1	RXD1
P52	-	GPIO	ANA	-	MISO	CC2	PG2	TXD1	RXD1
P54	-	GPIO	ANA	-	NSS(NSSO1)	SCL	PG4	TXD1	RXD1
P55	-	GPIO	ANA	-	NSS(NSSO2)	SDA	PG5	TXD1	RXD1

List of LED ports, analog ports, CONFIG configuration ports:

	GPIO(0)			ANA(1)				CONFIG
	LEDSEG	LEDCOM	LEDx	ADC	TOUCH	LCDCOM	LCDSEG	
P00	-	LEDCOM0	LED0	AN0	TK0	LCDCOM0		-
P01	-	LEDCOM1	LED1	AN1	TK1	LCDCOM1		-
P02	-	LEDCOM2	LED2	AN2	TK2	LCDCOM2		-
P03	-	LEDCOM3	LED3	AN3	TK3	LCDCOM3		-
P04	LEDSEG0	LEDCOM4	LED4	AN4	TK4	LCDCOM4	LCDSEG0	-
P05	LEDSEG1	LEDCOM5	LED5	AN5	TK5	LCDCOM5	LCDSEG1	-
P06	LEDSEG2	LEDCOM6	LED6	AN6	TK6	LCDCOM6	LCDSEG2	-
P07	LEDSEG3	LEDCOM7	LED7	AN7	TK7	LCDCOM7	LCDSEG3	-
P11	LEDSEG5	-	-	AN9	TK9		LCDSEG5	-
P12	LEDSEG6	-	-	AN10	TK10		LCDSEG6	-
P14	LEDSEG8	-	-	AN12	TK12		LCDSEG8	-
P15	LEDSEG9	-	-	AN13	TK13		LCDSEG9	-
P16	LEDSEG10	-	-	AN14	TK14		LCDSEG10	-
P17	LEDSEG11	-	-	AN15	TK15		LCDSEG11	-
P24	LEDSEG16			AN20	TK20		LCDSEG16	DSCK
P25	LEDSEG17			AN21	TK21		LCDSEG17	DSDA
P26	LEDSEG18			AN22	TK22		LCDSEG18	
P27	LEDSEG19			AN23	TK23		LCDSEG19	
P30				AN24	TK24		LCDSEG20	
P31				AN25	TK25		LCDSEG21	
P32				AN26	TK26		LCDSEG22	
P33				AN27	TK27		LCDSEG23	
P34				AN28	TK28		LCDSEG24	
P36				AN30	TK30		LCDSEG26	
P37				AN31	TK31		LCDSEG27	
P40	LEDSEG20			AN32	TK32		LCDSEG28	
P41	LEDSEG21			AN33	TK33		LCDSEG29	
P42	LEDSEG22			AN34	TK34		LCDSEG30	
P43	LEDSEG23			AN35	TK35		LCDSEG31	
P44	LEDSEG24			AN36	TK36		LCDSEG32	
P45	LEDSEG25			AN37	TK37		LCDSEG33	
P46	LEDSEG26			AN38	TK38		LCDSEG34	
P47	LEDSEG27			AN39	TK39		LCDSEG35	
P52	-	-	-	AN42	TK42			
P54	-	-	-	AN44	TK44			OSCOUT
P55	-	-	-	AN45	TK45			OSCIN

Note: The chip pins are subject to the actual chip.

4. Feature Summary

4.1 System Clock

The system clock has four clock sources, which can be selected by setting the system configuration register or user register. The system clock module has the following features:

- Selectable internal high-speed oscillation HSI (48MHz).
- Optional external high-speed crystal oscillation HSE (8MHz/16MHz).
- Optional external low-speed crystal oscillation LSE (32.768KHz).
- Optional internal low-speed oscillation LSI (125KHz).
- Any two clock sources can be switched to each other (switching is prohibited between HSE and LSE).
- External high-speed and low-speed oscillators provide a stop-oscillation monitoring function (SCM) when the system clock is provided.

4.2 Reset

The reset operation is used to initialize the internal circuitry of the chip, allowing the system to start working from a determined state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low voltage reset.
- CONFIG status protection reset.
- Power-on configuration monitor reset.
- Watchdog overflow reset.
- Window watchdog overflow reset.
- Software reset.

Any of the above reset situations require a certain response time, and the system provides a perfect reset process to ensure the smooth progress of the reset operation.

4.3 Interrupt Control

The chip has multiple interrupt sources and interrupt vectors, user-programmable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer (SCM), PWM, I2C, SPI, UART0/1/2, P0/P1/P2/P3/P4/P5, ADC, LVD, etc the actual number of LED, LCD, TOUCH, WWDT, interrupt sources varies depending on the product.

The chip specifies two interrupt priorities, allowing for two levels of interrupt nesting. When an interrupt has already responded, if a high-level interrupt is requested, the latter can interrupt the former, realizing interrupt nesting.

4.4 Power Management

4.4.1 Working Mode

The chip has 3 different operating modes to adapt to the power consumption requirements of different applications.

- Normal operating mode: The MCU is in normal working condition and the peripherals are operating normally.
- Idle mode IDLE: The MCU is in idle mode, the CPU stops working, and the peripherals are running normally. This mode can be woken up by any interrupt.
- Hibernate mode STOP: The MCU is in sleep mode, the CPU stops working, and the peripherals stop working. This mode can be woken up by INT0/1 interrupt, GPIO interrupt wake-up, WUT timed wake-up, LSE timed wake-up, and WWDT timed wake-up.

4.4.2 Power Supply Low Voltage Reset (LVR)

When the supply voltage falls below the set sense voltage, the system resets.

There are four options for low-voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.4.3 Power Supply Low Voltage Detection (LVD)

The low voltage detection circuit compares the supply voltage to the set voltage and generates an interrupt request signal if the supply voltage is lower than the set voltage.

The programmable detection voltage range is 2.0V to 4.3V, and a total of 8 levels are available.

4.5 Timer

4.5.1 WDT Timer

The watchdog timer is an on-chip timer that is provided by the system clock and overflows with WDT timing will produce a reset. Watchdog reset is a protective setting of the system, when the system is running to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an indefinite dead loop. WDT timers have the following features:

- Watchdog overflow time 8 levels optional.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 WWDT Timer

The Window Watchdog Timer is an on-chip timer with window comparison time selectable and clock source provided by LSI. Window watchdog overflow reset is a protection setting of the system, when the system is running to an unknown state, the window watchdog can be used to reset the system, thereby avoiding the system from entering an indefinite cycle. WWDT has the following features:

- WWDT prescale 15 levels are selectable.
- The watchdog reset enable and watchdog reset flag can be set.
- The 5-bit WWDT comparison value is configurable.
- The WWDT overflow force reset enable can be software configured.
- Two WWDT modes are available (Window Dog Feeding Mode/ Any Time Dog Feeding Mode).
- WWDT sleep wake-up enable can be set.

4.5.3 Timer Counter 0/1 (Timer0/1)

Timer 0 is similar in type and structure to Timer 1 and is two 16-bit up counting timers. Timer0 has 4 modes of operation and Timer1 has 3 modes of operation, which provide basic timing and event counting operations.

In "timer mode", the timing register is incremented every 12 or 4 system cycles when the timer clock is enabled. In "counter mode", the timing register increments whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated Timer functions.
- External counting function can be implemented.
- Can be used for gated counting functions.
- The counter overflow interrupts.

4.5.4 Timer Counter 2 (Timer2)

Timer 2 is a 16-bit timer that can be used for the generation of various digital signals and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following features:

- Can be used as a normal timer.
- Can be used for gated Timer functions.
- External counting function can be implemented.
- It has the functions of reload prohibition, overflow automatic reload, and automatic reloading of external pin falling edge.
- Capture can be triggered by the rising edge, falling edge, double edge, or low byte of the write capture register.
- Features a comparison function that generates a periodic signal with a controllable duty cycle of the PWM waveform.
- Timing, external triggering, capture, and comparison can all produce interrupts.

4.5.5 Timer 3/4 (Timer3/4)

Timer 3/4 is similar to timer 0/1 in that it is two 16-bit timers. Timer3 has 4 working modes and Timer4 has 3 working modes. In contrast to Timer0/1, Timer3/4 only provides timer operations.

With the timer activated, the value of the register is incremented every 12 or 4 system cycles.

4.5.6 LSE Timer (LSE_Timer)

The LSE timer is a clock source from an external low-speed clock LSE, a 16-bit up-counting timer. LSE timers have the following features:

- Timer function.
- A 16-bit timer value can be set.
- Works in sleep mode.
- An interrupt can occur when the count value is equal to the timer value.
- A timed interrupt wakes up idle mode/sleep mode.

4.5.7 Wake-up Timer (WUT)

The WUT wake-up timer is a clock source from the internal low-speed clock LSI, a 12-bit, up-count timer for sleep wake-ups. After the system enters sleep mode, the CPU stops working with all peripheral circuitry, and the internal low-speed clock LSI provides a clock to the WUT counter. WUT has the following features:

- The system can be woken up at a configured time during sleep.
- The counting clock is available in divide-by-1, 8, 32, and 256.
- A 12-bit timer value can be set.

4.5.8 Baud Rate Generator (BRT)

The BRT timer is a 16-bit baud rate timer whose clock source comes from the system clock and primarily provides a clock for the UART module. BRTs have the following features:

- Has an independent control switch.
- The counting clock has an 8-levels frequency division option.
- 16-bit increment count.

4.6 Enhanced Digital Peripherals

4.6.1 Cyclic Redundancy Check Unit (CRC)

Cyclic redundancy check CRC is the most commonly used error check code in the field of data communication, which is characterized by the length of the information field and the check field can be arbitrarily selected. The chip CRC check unit generates polynomials using "$X^{16}+X^{12}+X^5+1$" (CRC16-CCITT) to program the data to be verified, so that the module is not limited to the code flash memory area and can be used for multi-purpose checks.

4.6.2 Buzzer Driver (BUZZER)

The buzzer drive module consists of an 8-bit counter, clock driver, control register, and a square wave with an output duty cycle of 50% and a frequency covering a wide range. BUZZER has the following features:

- Has a separate enable control switch.
- The clock division ratio of 8, 16, 32, and 64 can be set.
- The output frequency is 8-bit controllable, and the output can be set (1~255) x 2 frequency division.

4.6.3 PWM Module

The PWM module supports 6-channel PWM generators with independently programmable cycles and duty cycles. PWM has the following features:

- Supports two kinds of waveform outputs in single-shot and continuous mode.
- Supports four control modes: independent, complementary, synchronous, and group control.
- The counting clocks are available in divide-by-1, 2, 4, 8, and 16.
- Edge alignment mode is supported.
- Supports dead-zone programming.
- Output polarity can be set.
- Supports downward comparison and zero point interrupt.

4.7 Display Interface

4.7.1 Hardware LCD Driver Module

The LCD driver module contains a controller, a duty cycle generator, COM and SEG outputs. The module has the following features:

- Up to 8 COM ports, 23 SEG ports.
- Supports both traditional resistor and fast charging modes.
- Fast charging time is selectable.
- Contrast adjustment is supported.
- Bias voltage selectable: 1/2, 1/3, 1/4.
- Duty cycles selectable: 1/4, 1/5, 1/6, 1/8.
- Selectable clock sources: system clock, LSI, LSE.
- Supports driving LCD in sleep mode.

4.7.2 Hardware LED Matrix Driver Module

The hardware LED matrix driver module can easily realize the display driver of the LED. The module has the following features:

- 1/4, 1/5, 1/6, 1/8 DUTY is available.
- Three clock sources are available: system clock, LSI, and LSE.
- 16-bit clock source frequency division controller.
- COM port common-negative, common-positive two drive mode optional.
- Supports up to 8 COM ports and 20SEG ports.
- Each COM and SEG port has an enable control bit.
- COM port current 55mA, 220mA available (V_{OL} = 1.5V@VDD = 5 V).
- The SEG port current is selectable in 16 levels and the maximum current can reach 50mA (V_{OH}=3.5V@VDD=5V).

4.7.3 Hardware LED Dot Matrix Driver Module

The hardware LED dot matrix driver module can easily realize the LED dot matrix driver. The module has the following features:

- Up to 8 LED0-LED8 pin enables are available.
- Supports up to 56 led drivers, with dot matrix 4x4, 5x5, 6x6, 6x7, 7x7, 7x8.
- Each lamp supports two on-time options, each with a 16-bit timing setting.
- Each lamp display data is selectable.
- System clock source, LSI, LSE three selection.
- 16-bit clock source frequency division controller.
- Both cyclic scan mode and interrupt scan mode are supported.
- Current 16 levels are available for a maximum current of 50 mA (V_{OH}=3.5V@VDD=5V).

4.8 Communication Module

4.8.1 SPI Module

The SPI is a fully configurable SPI master/slave device that allows the user to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it is also capable of interprocessor-to-processor communication in multi-host systems. SPI has the following features:

- Full-duplex synchronous serial data transfer.
- Supports master/slave mode.
- Support for multi-host systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock (F_{SYS}≤24MHz).
- The bit rate produces 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Four transmission formats are supported.
- Send/receive completion can produce an interrupt.

4.8.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and efficient connection for data exchange between the microprocessor and the I2C bus. The I2C module has the following features:

- Support 4 working modes: master transmission, master reception, slave transmission, slave reception.
- Supports 2 transfer speed modes:
  Standard (up to 100Kb/s);
  Fast (up to 400Kb/s).
- Perform arbitration and clock synchronization.
- Support for multi-host systems.
- The host mode supports7-bit addressing mode and 10-bit addressing mode on the I2C-bus (software supported).
- Slave mode supports7-bit addressing mode on the I2C-bus.
- Allows operation over a wide clock frequency range (built-in 8-bit timer).
- Receive/send completion can produce an interrupt.

4.8.3 UARTn Module

The UARTn module contains UART0/UART1 /UART2, 3 serial ports with exactly the same functions. UARTn has the following features:

- Full-duplex serial port.
- Synchronous mode is supported.
- Supports 8-bit asynchronous transceiver mode with variable baud rate.
- Supports a 9-bit asynchronous transceiver mode with variable baud rate
- Baud rates can be generated by timer1/Timer4/Timer2/BRT modules.
- Send/receive completion can produce an interrupt.

4.9 Analog Module

4.9.1 Analog-to-digital Converter (ADC)

The ADC module is a 12-bit successive approximation analog-to-digital converter. After the port analog input signal is multiplexed, it is connected to the sample-and-hold circuitry of the analog-to-digital converter, which generates a 12-bit binary result based on the input analog signal and saves the result in the ADC result register. ADC has the following characteristics:

- Up to 30 external channels.
- The ADC can be set to average 1/4/8/16 conversions.
- The ADC conversion clock is available in 15 clock dividers.
- The ADC reference voltage can be selected from VDD/1.2V/2.0V/2.4V/3.0V.
- Supports external port edges, PWM trigger ADC conversion.
- Supports ADC conversion result comparison output.
- Supports interrupt generation when an ADC conversion is complete.

4.9.2 Touch Module (TOUCH)

The touch module is an integrated circuit designed to realize the human touch interface, which can replace the mechanical light touch button to achieve waterproof and dustproof, sealed isolation, strong and beautiful operation interface.

Technical parameters:

- Up to 30 touch buttons are available.
- No external touch capacitors are required.
- The effective touch response time is less than 100ms.

4.10 FLASH Memory

The FLASH memory contains program memory (APROM/BOOT) and non-volatile data memory (Data FLASH) that can be accessed by the associated special function register (SFR) to achieve IAP functionality. Flash memory supports the following operations:

- Byte read operation.
- Byte write operations.
- Page erase operation.
- FLASH space CRC check operation.

4.11 Unique ID (UID)

Each chip has a 96-bit unique identification number, known as Unique identification. The UID is already set at the factory and cannot be modified by the user.

5. User Configuration

The System Configuration Register (CONFIG) is a FLASH option for the initial conditions of the MCU and cannot be accessed or operated by the program. The System Configuration Register allows you to set the following:

- The way watchdogs work.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset voltage.
- Debug mode disable or enable.
- Oscillation mode, prescale selection.
- Internal high-speed oscillator frequency division selection.
- External crystal oscillator selection.
- Sleep wake-up wait time.
- APROM/BOOT space.

6. Electrical Parameters

6.1 Absolute Maximum Rating

symbol	parameter	minimum	maximum	unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Supply voltage	-0.3	5.8	V
V_{AND}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	300	mA
THE_{IOs}	Maximum sink current for a single IO	-	55	mA
	Maximum Sink Current for a Single IO (LED COM)	-	220	mA
	Maximum current for a single IO	-	50	mA
	Single IO Maximum Current Pull (LED SEG)	-	50	mA
	Maximum sink current for all IO	-	300	mA
	Maximum pull current for all IO	-	120	mA

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V，T_A=25℃

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
VDD	Operating voltage	F_{SYS} = 48MHz, machine cycle = 2T F_{SYS} = 8MHz ~ 24MHz, machine cycle = 1T	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals off Machine cycle = 2T	-	7	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off Machine cycle = 2T	-	7	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off Machine cycle = 1T	-	5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off Machine cycle = 1T	-	5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off Machine cycle = 1T	-	4	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off Machine cycle = 1T	-	4	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off Machine cycle = 1T	-	3	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off Machine cycle = 1T	-	3	-	mA
		VDD=5V, F_{SYS}=32.7678KHz, all peripherals off Machine cycle = 1T	-	0.26	-	mA
		VDD=3V, F_{SYS}=32.7678KHz, all peripherals are off Machine cycle = 1T	-	0.23	-	mA
	IDLE mode	VDD=5V, F_{SYS}=48MHz, all peripherals off	-	5.5	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off	-	5.5	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off	-	3.5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	3.5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	2.5	-	mA

		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	2.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	2	-	mA
		VDD=5V, F_{SYS}=32.768KHz, all peripherals are off	-	0.26	-	mA
		VDD=3V, F_{SYS}=32.768KHz, all peripherals are off	-	0.23	-	mA
I_{SLEEP1}	Sleep current	All peripherals are off and the LSE timer is enabled	-	20	-	uA
I_{SLEEP2}	Sleep current	All peripherals are off and LSI, WUT timers are enabled	-	7	-	uA
I_{SLEEP3}	Sleep current	All peripherals are turned off	-	6	-	uA
I_{LI}	Input leakage	-	-	-	0.1	uA
V_{IL}	Enter a low level	-	VSS	-	0.3VDD	V
V_{IH}	Enter high	-	0.7VDD	-	VDD	V
V_{OL}	Output low voltage	VDD=5V, I_{OL1}=18mA	-	-	0.4	V
		VDD=5V，I_{OL2}=55mA (LED COM)	-	-	0.4	V
		VDD=3V, I_{OL1}=12mA	-	-	0.4	V
		VDD=3V，I_{OL2}=44mA (LED COM)	-	-	0.4	V
V_{OH}	Output high voltage	VDD=5V, I_{OH1}=50mA	3.5	-	-	V
		VDD=5V, I_{OH2}=50mA (LED SEG Max)	3.5	-	-	V
		VDD=5V, I_{OH3}=5mA (LED HIMSELF Min)	3.5	-	-	V
		VDD=3V, I_{OH1}=20mA	2.1	-	-	V
		VDD=3V, I_{OH2}=20mA (LED SEG Max)	2.1	-	-	V
		VDD=3V, I_{OH3}=2mA (LED MIN)	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-up and Power-down Operation

T_A= 25°C, excluding 32.768K crystal resonant time

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	2	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	2	-	-	us/V

6.3.2 External Oscillator

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{HSE}	Operating voltage	F=8/16MHz,C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz,C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

symbol	parameter	Test conditions	Frequency error	minimum	Typical	maximum	unit
F_{HSI}	Internal high speed 48MHz	T_A=0℃ to 80℃	±1%	-	48	-	MHz
		T_A=-40℃ to 105℃	±2%	-	48	-	MHz
F_{LSI}	Internal low speed 125KHz	T_A=25℃	±3%	-	125	-	KHz
		T_A=-40℃ to 105℃	±5%	-	125	-	KHz

6.3.4 Low-voltage Reset Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 LVD Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVD1}	Low pressure detection threshold 2.00V	1.90	2.00	2.10	V
V_{LVD2}	Low pressure detection threshold 2.20V	2.10	2.20	2.30	V
V_{LVD3}	Low pressure detection threshold 2.40V	2.30	2.40	2.50	V
V_{LVD4}	Low pressure detection threshold 2.70V	2.60	2.70	2.80	V
V_{LVD5}	Low pressure detection threshold 3 00V	2.90	3.00	3.10	V
V_{LVD6}	Low pressure detection threshold 3 70V	3.60	3.70	3.80	V
V_{LVD7}	Low pressure detection threshold 4 00V	3.90	4.00	4.10	V
V_{LVD8}	Low pressure detection threshold 4 30V	4.20	4.30	4.40	V

6.4 FLASH Electrical Parameters

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	27	105	℃
$N_{ENDURANCE}$	The number of erases and writes	Program FLASH	20000	-	-	Cycle
		Data Flash	100,000			Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{PROG}	Programming time	-	-	7	-	us
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming the current	-	-	-	3.6	mA
I_{DD3}	Erase the current	-	-	-	2	mA

6.5 Simulation Characteristics

6.5.1 BANDGAP Electrical Characteristics

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{BG}	Internal reference 1.2V	VDD=2.1~5.5V、T_A=-40°C to 105°C	1.182	1.2	1.218	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

symbol	parameter	minimum	Typical	maximum	unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF1}	Reference voltage 1	-	IN_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (non-V_{BG}).	1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3	1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4	2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5	2.985	3.0	3.015	V
V_{ADI}	Input voltage	0	-	V_{REF}	V
N_R	resolution	12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us).	±1			LSB
INL	Integral nonlinearity error (V_{REF} =V_{AVDD}=5V, T_{ADCK}=0.5us).	±2			LSB
T_{ADCK}	ADC clock cycle	0.25	-	32	us
T_{SMP}	ADC sampling time	4	-	8	T_{ADCK}
T_{CONV}	ADC conversion time	-	12	-	T_{ADCK}
T_{ADC}	ADC sampling conversion time (T_{ADC} = T_{SMP} + T_{CONV}).	16	-	20	T_{ADCK}
F_S	sample rate(V_{REF}=V_{AVDD}=5V)	-	-	250	Ksps

6.6 EMC Features

6.6.1 EFT Electrical Characteristics

symbol	parameter	Test conditions	maximum	unit	grade
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25°C, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4800	V	4B

Note: The immunity performance of electrical fast transient pulse swarm (EFT) is closely related to the system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.). The EFT parameters in the table above are measured on the CMS internal test platform and are not suitable for all application environments, and the test data is for reference only. All aspects of the system design may affect the EFT performance, in the application of high EFT performance requirements, the design should pay attention to avoid interference sources affecting the operation of the system, it is recommended to analyze the interference path and optimize the design to achieve the best immunity performance.

6.6.2 ESD Electrical Characteristics

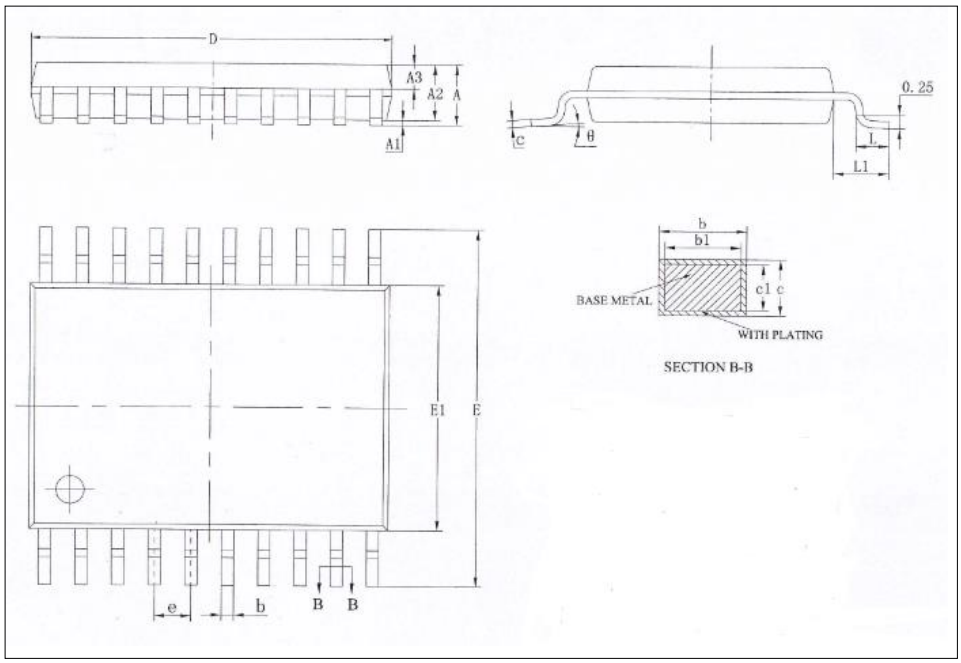
symbol	parameter	Test conditions	maximum	unit	grade
V_{ESD}	Electrostatic discharge (Human discharge mode HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	8000	V	3B
	Electrostatic discharge (Machine discharge mode MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	400	V	C

6.6.3 Latch-Up Electrical Characteristics

symbol	parameter	Test conditions	The test type	minimum	unit
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)	±200	mA

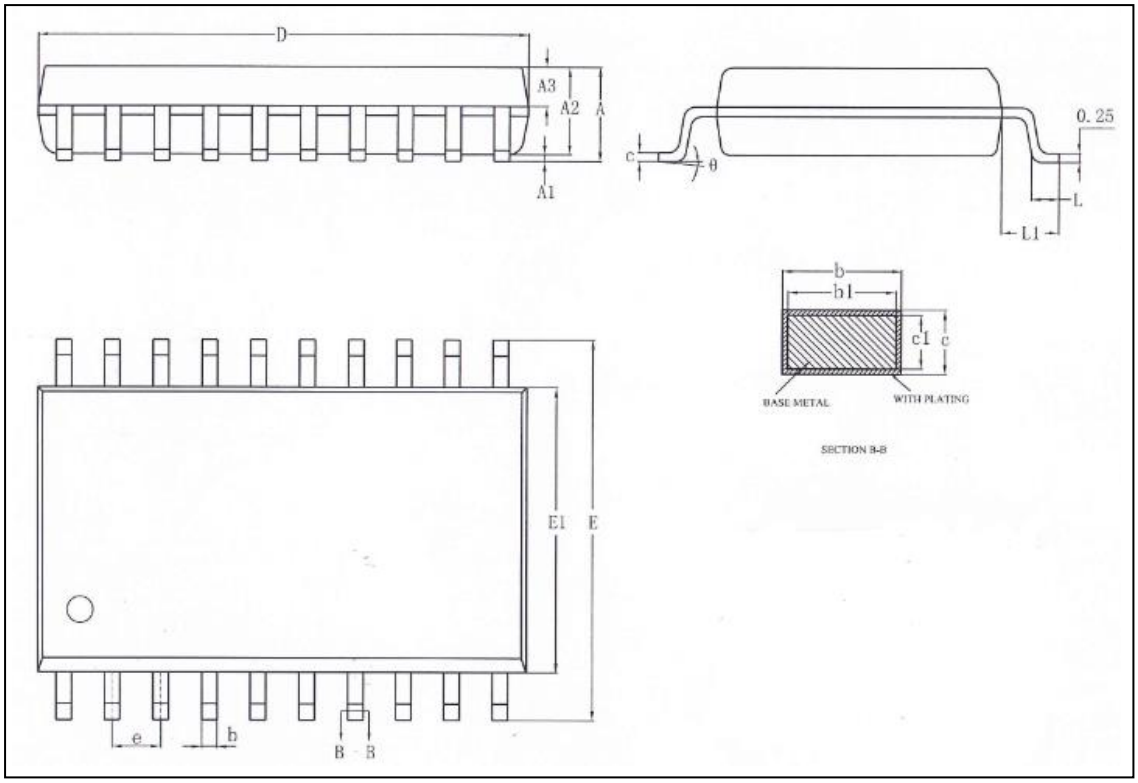
7. Packaging information

7.1 TSSOP20



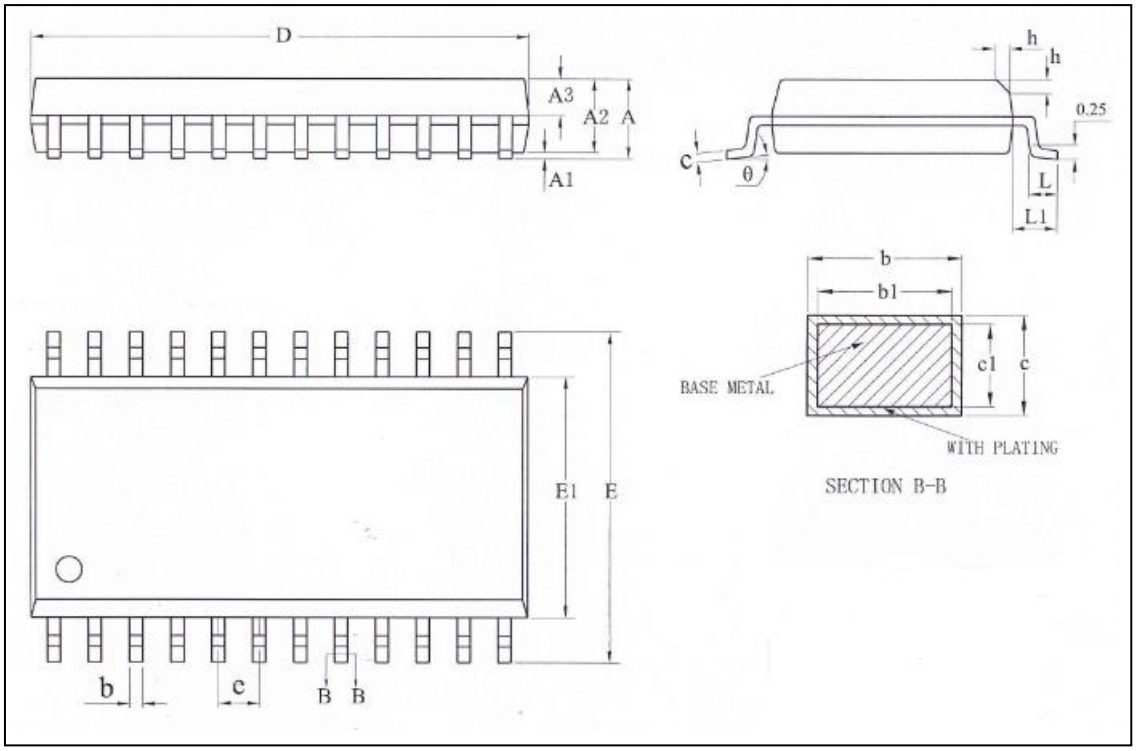
Symbol	Millimetre		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

7.2 SOP20



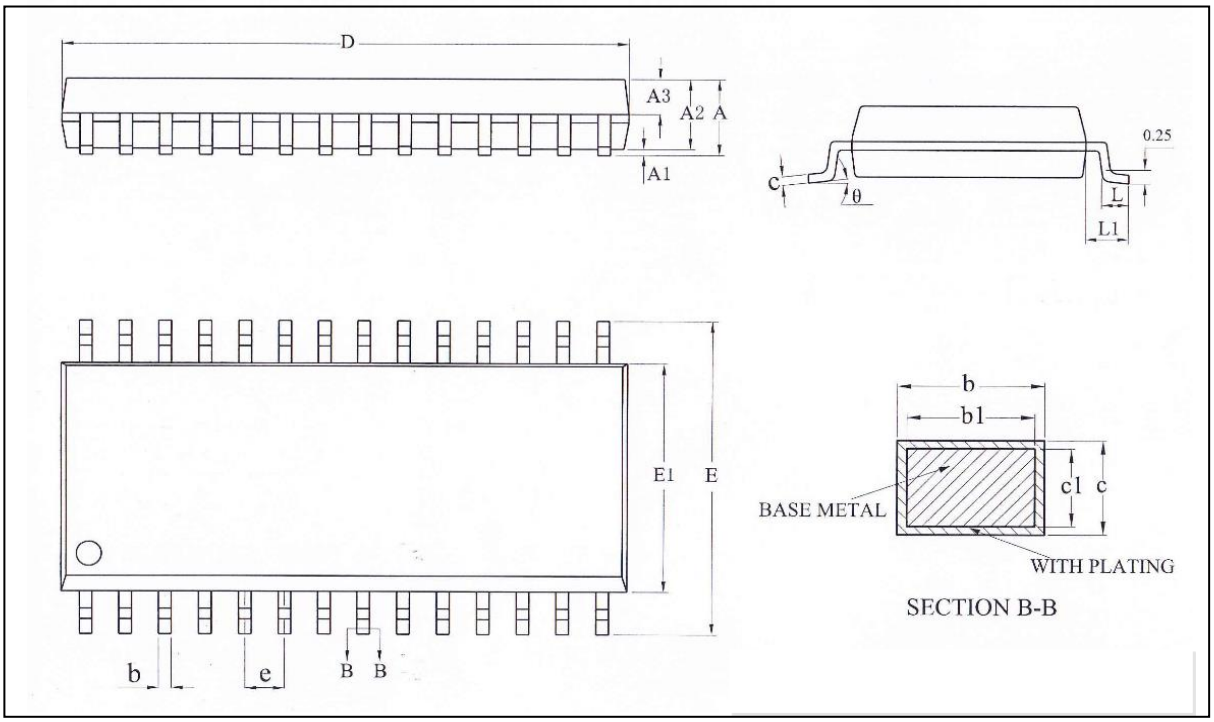
Symbol	Millimetre		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	-	0.43
b1	0.34	0.37	0.40
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.3 SOP24



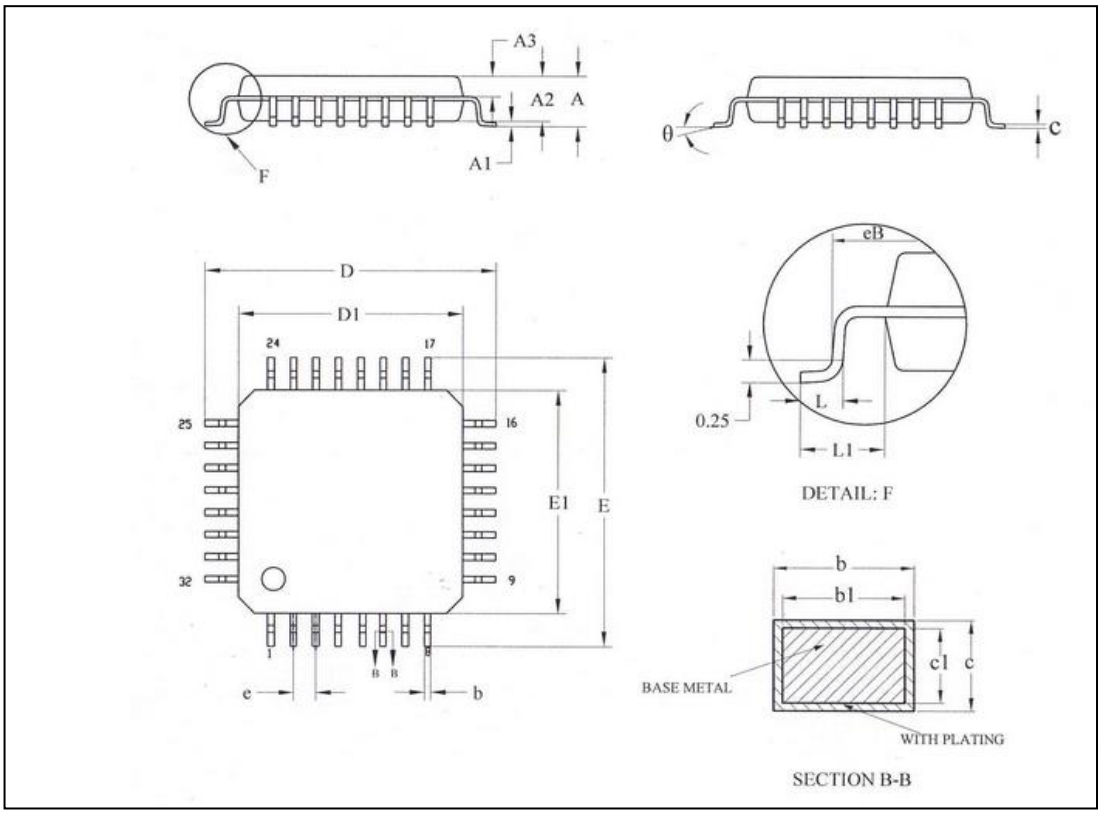
Symbol	Millimetre		
	Min	Nom	Max
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
A2	2.26	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.40
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.4 SOP28



Symbol	Millimetre		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.5 LQFP32



Symbol	Millimetre		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.25
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.40	-	0.65
L1	1.00REF		
θ	0°	-	7°

8. Version History

The version number	Time	Revision content
V1.00	August 2020	Initial release